MS-7524 VER:0A

CPU:

Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

North Bridge - Intel Eagle Lake P45/G45
North Bridge - Intel ICH10

On Board Chipset:

Clock Gen - SLG8XP548
LPC Super I/O - Fintek F71882F
LAN - Intel82567
Audio Codec - ALC888
1394 Controller - JMB381
SATA Controller - JMB363

Main Memory:

DDR 2*4(Max4GB)

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

PWM:

Intersil ISL6333 (3 Phases)

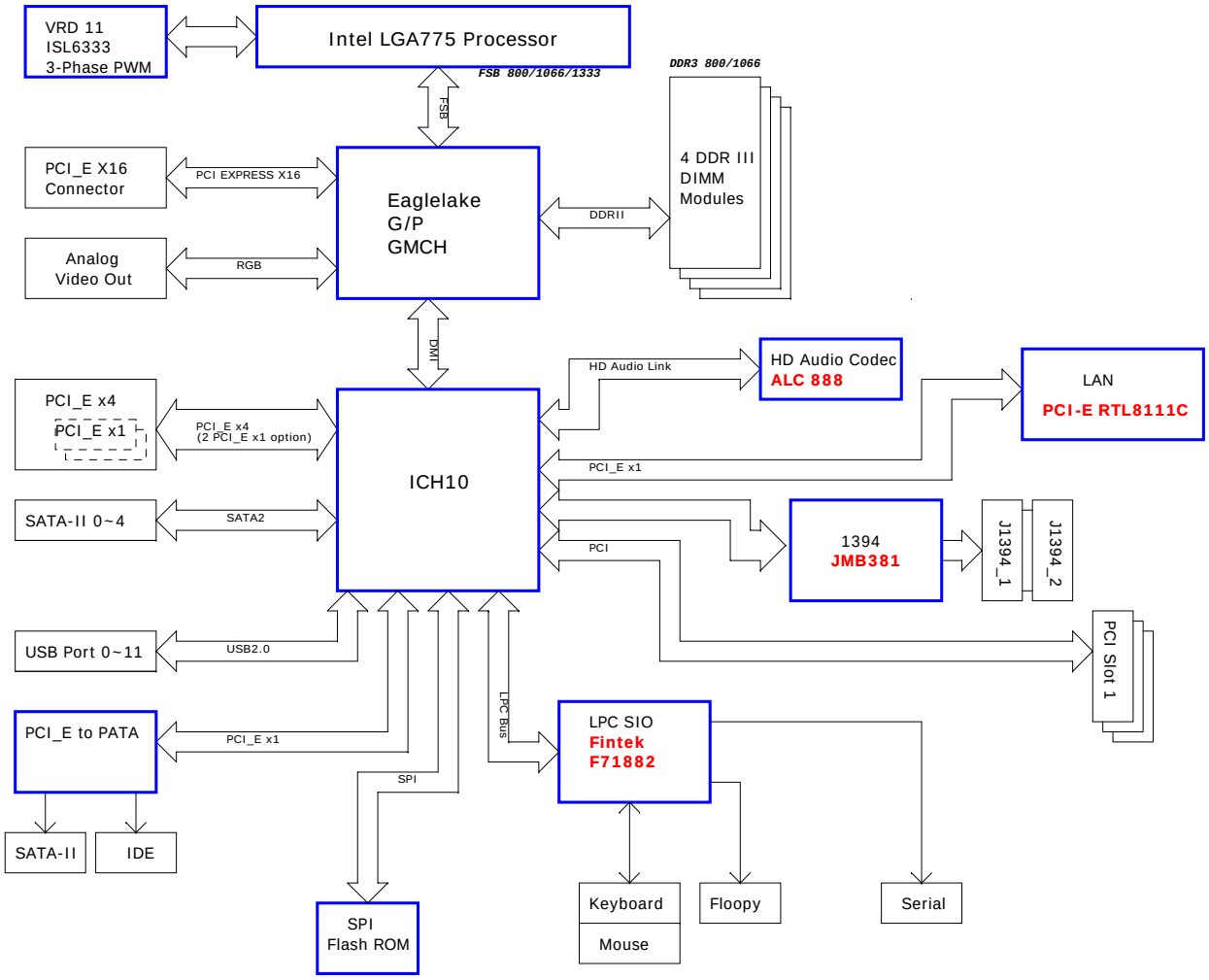
MICRO-START INT'L CO.,LTD.

Title: Cover Sheet

Size: C | Document Number: MS-7524M1 | Rev: 0A

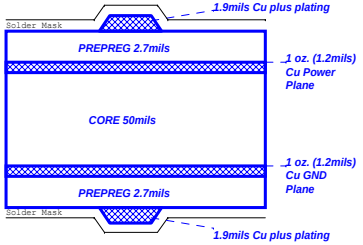
Date: Thursday, December 27, 2007 | Sheet 1 of 42

Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

MICRO-START INT'L CO.,LTD.

Title: Block Diagram

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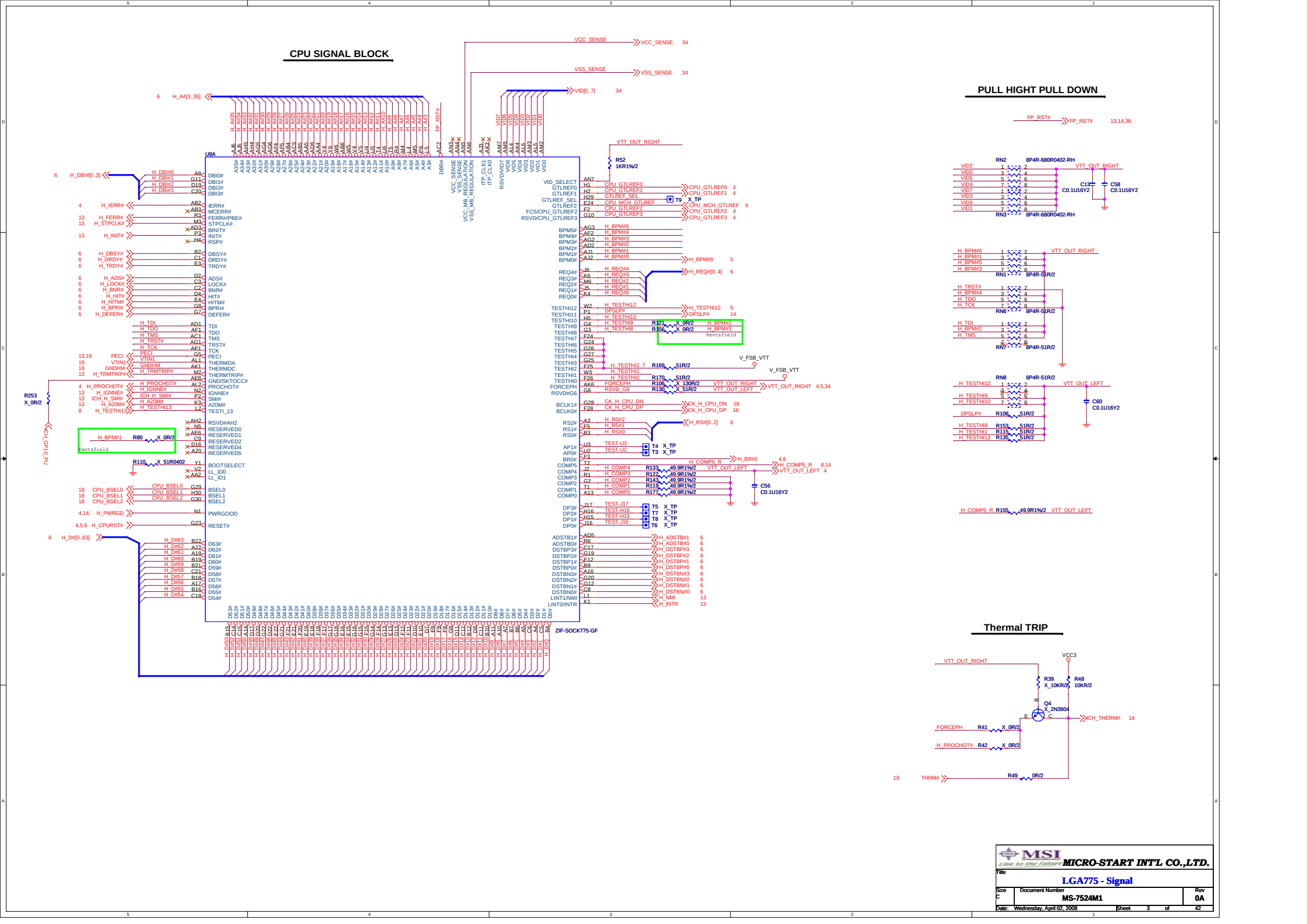
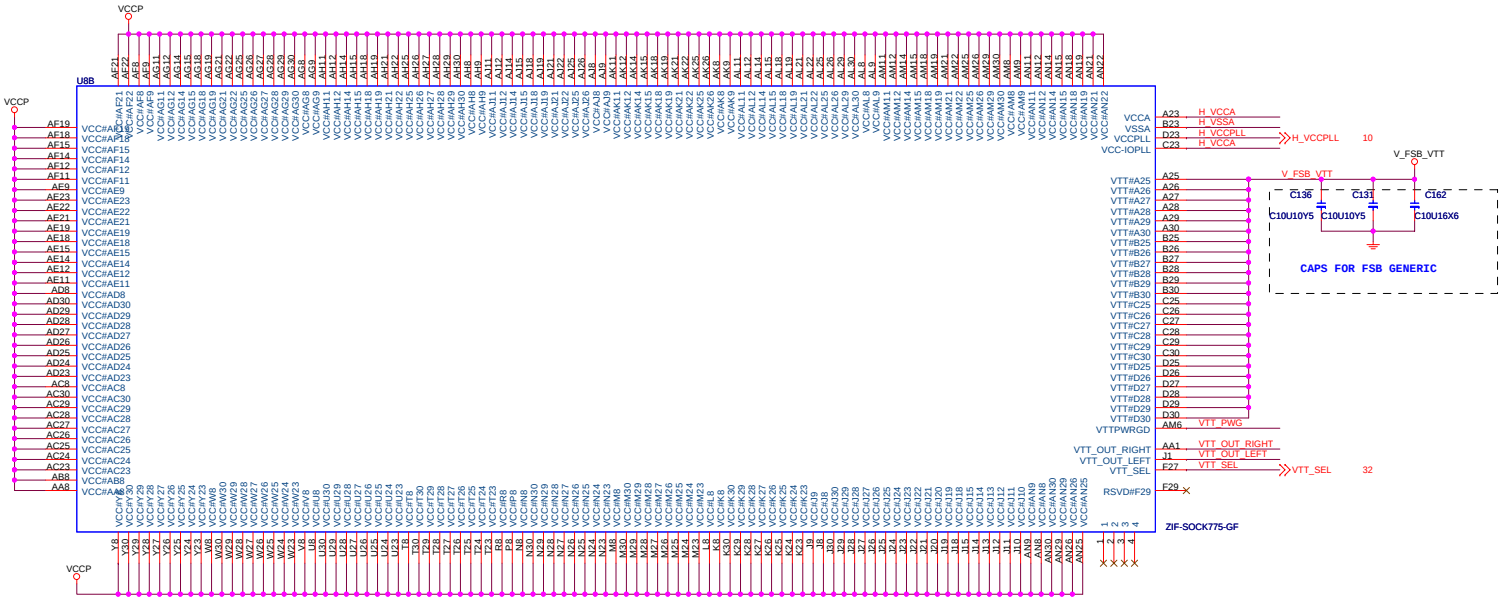
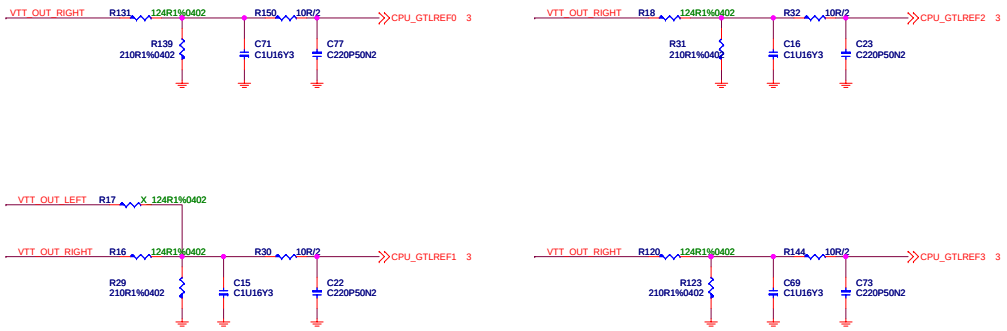

CPU SIGNAL BLOCK
PULL HIGHT PULL DOWN
Thermal TRIP
U8A
ZIF-SOCK775-GF
VCC_SENSE
VSS_SENSE
VID[0..7]
H_A#[3..35]
H_D#[0..63]
H_DBI#[0..3]
FP_RST#
VTT_OUT_RIGHT
V_FSB_VTT
VTT_OUT_LEFT
MICRO-START INT'L CO.,LTD.
LGA775 - Signal
MS-7524M1
0A
Wednesday, April 02, 2008
Sheet 3 of 42

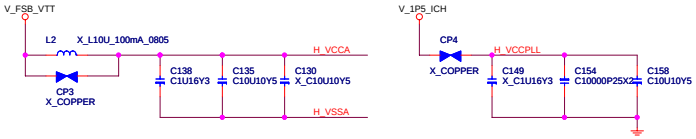


CPU	CPU_GTLREF1_SEL	GTL VOLTAGE
KENTSFIELD FSB OVERCLOCKING	0	0.685 VTT
ALL OTHER CPUS	1	0.630 VTT

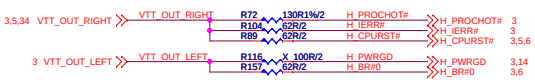
***GTLREF VOLTAGE SHOULD BE**
0.67 * VTT = 0.8V (At VTT=1.2V)



***PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET**
***TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS**

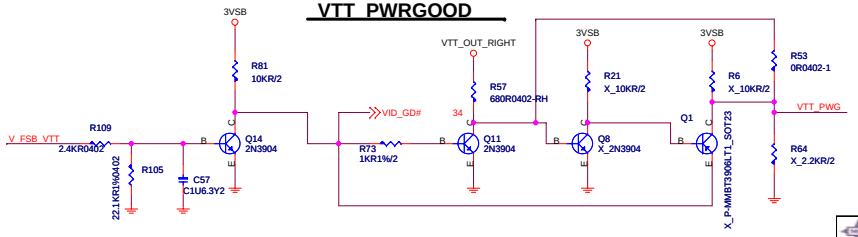


PLACE AT CPU END OF ROUTE



VR Configuration	Iccmax	VR TDC	Dynamic Icc	RLL	TOB	Maximum VID
775_VR_CONFIG_04A	78 A	68 A	55 A	1.40 mΩ	+/-25 mV	1.4 V
775_VR_CONFIG_04B	119 A	101 A	95 A	1.00 mΩ	+/-19 mV	1.4 V
775_VR_CONFIG_05A	100 A	85 A	65 A	1.00 mΩ	+/-19 mV	1.4 V
775_VR_CONFIG_05B	125 A	115 A	95 A	1.00 mΩ	+/-19 mV	1.4 V
775_VR_CONFIG_06	75 A	60 A	50 A	1.00 mΩ	+/-19 mV	1.425 V

VTT_PWRGOOD



MSI Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **LGA775 - Power**

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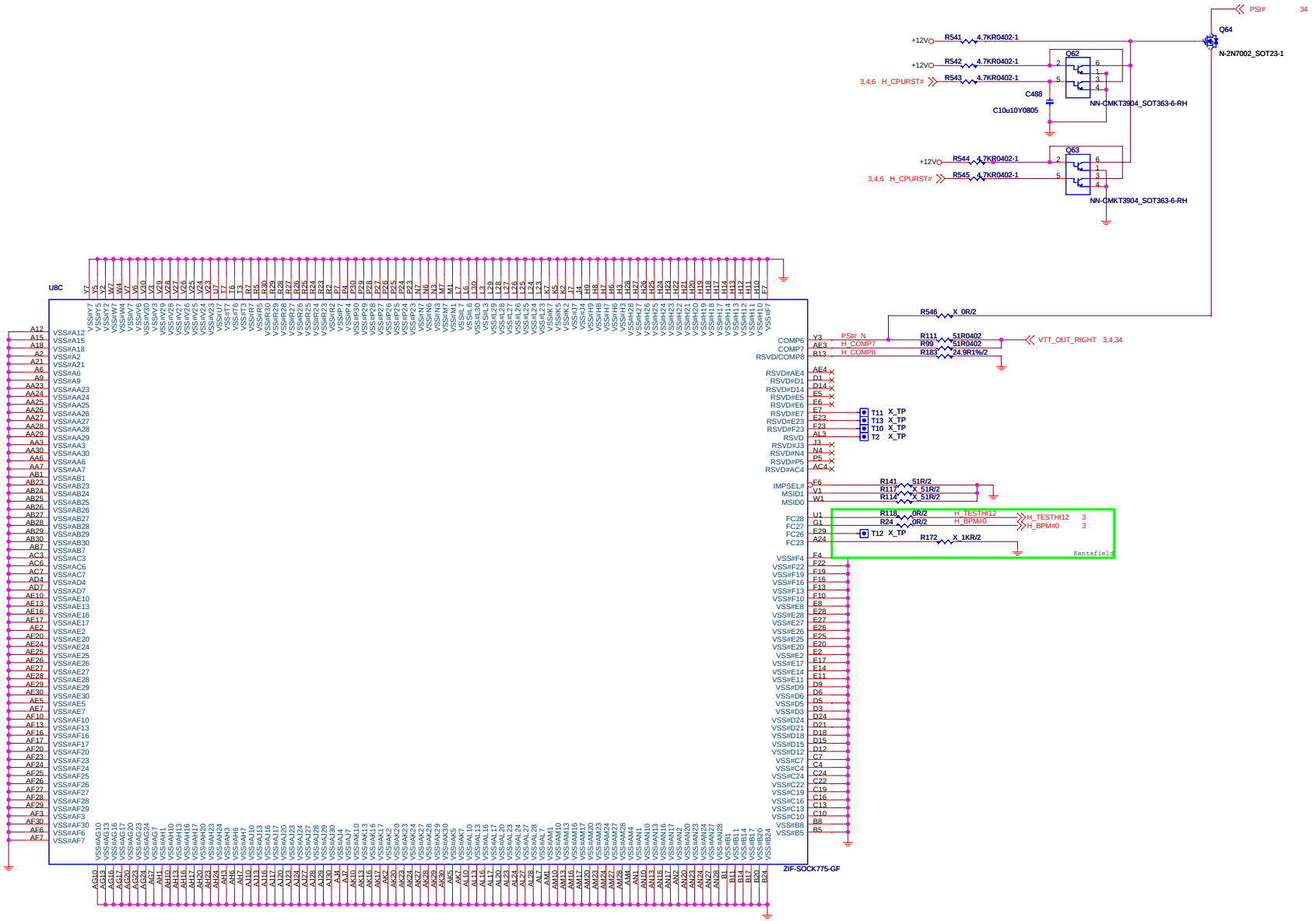
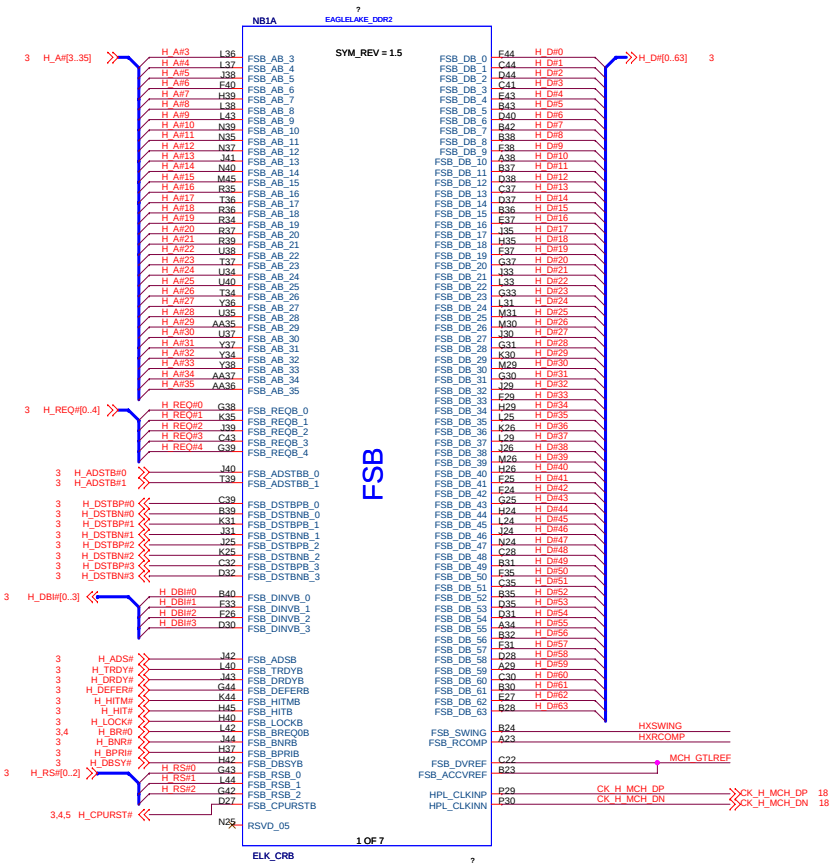


MSI MICRO-STAR INT'L CO.,LTD.			
Title: LGA775 - GND			
Size: C	Document Number: MS-7524M1		Rev: 0A
Date: Wednesday, April 02, 2008	Sheet 5 of 42		

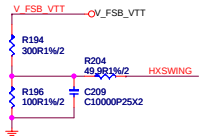


Really need or just reserve the invert?

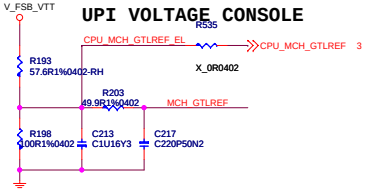
PIN	H	L	Description
MTYPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TCEN	Enable	Disable	TLS confidentiality

***GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.8V (At VTT=1.2V)**

HXSWING SHOULD BE 1/4*VTT



UPI VOLTAGE CONSOLE



R225, R226 is from changingof the demo board

MSI MICRO-STAR INT'L CO.,LTD.

Title: Eagle - FSB

Size	Document Number	Rev
C	MS-7524M1	0A

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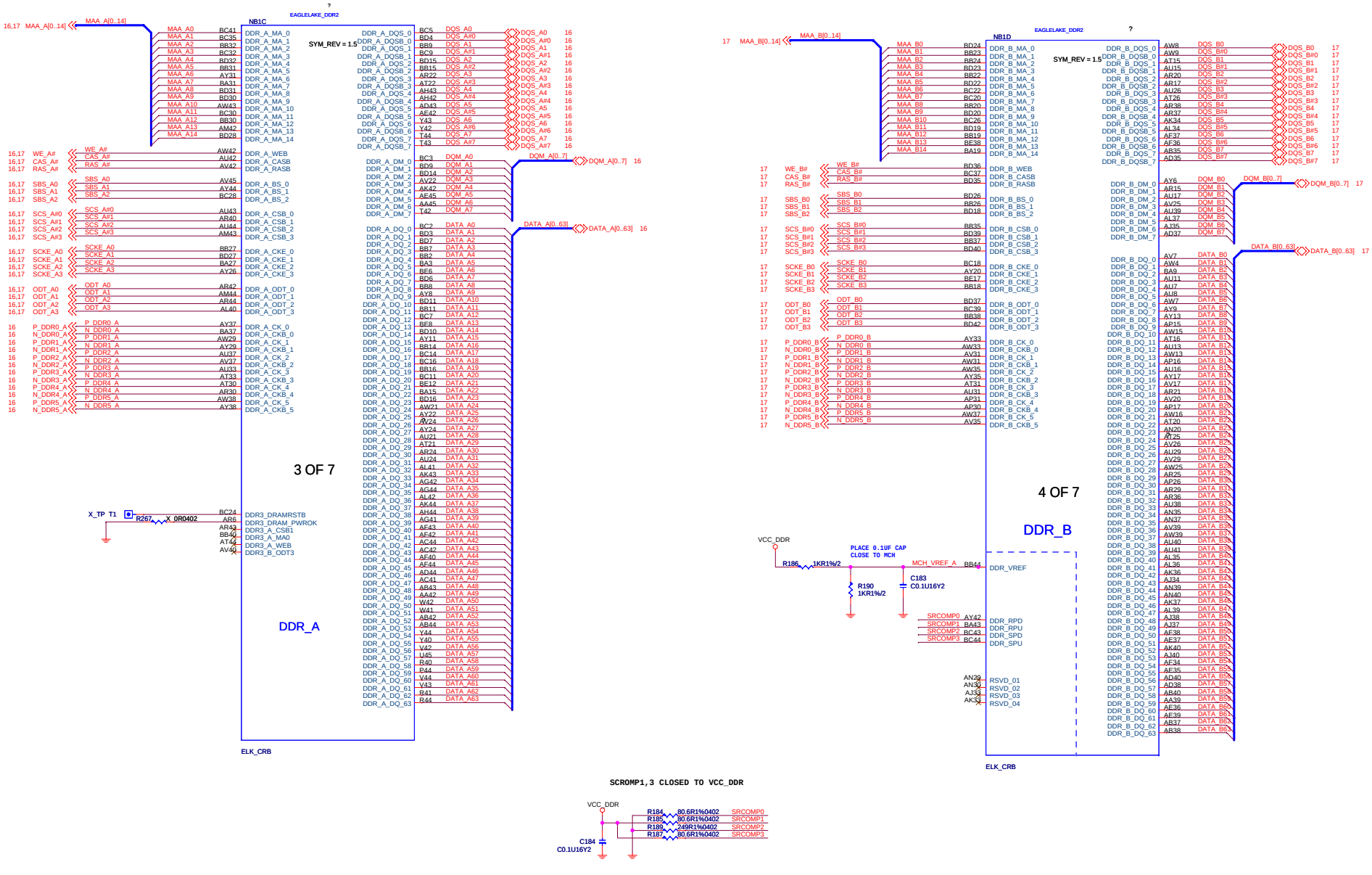
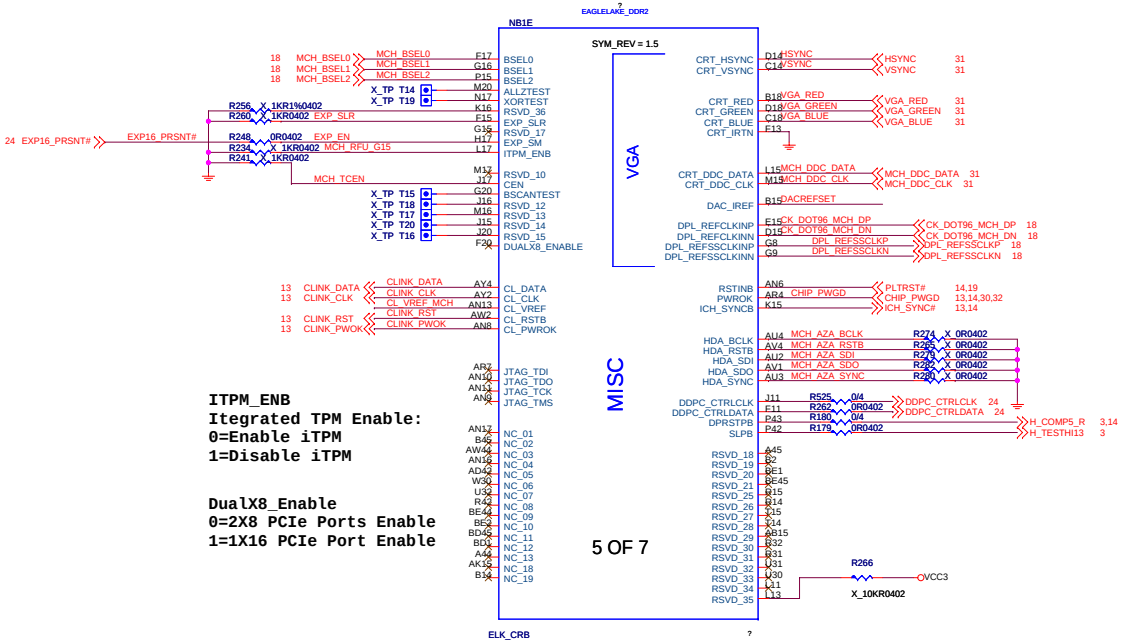
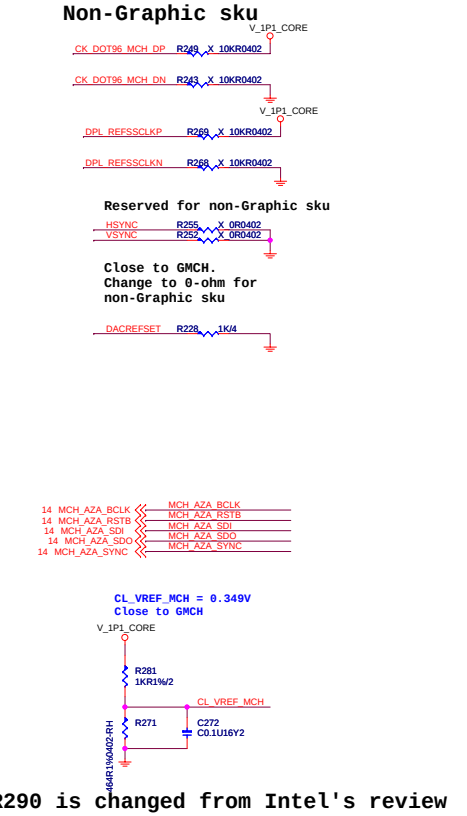

NB1C
EAGLELAKE_DDR2
SYM_REV = 1.5
3 OF 7
DDR_A
ELK_CRB
NB1D
4 OF 7
DDR_B
SCROMP1,3 CLOSED TO VCC_DDR
PLACE 0.1UF CAP CLOSE TO MCH
MICRO-START INT'L CO.,LTD.
Eagle - Memory DDR2
MS-7524M1
0A
Wednesday, April 02, 2008





R290 is changed from Intel's review

100MHz Clock Group (DPL_REFSSCLKINP/ DPL_REFSSCLKINN)

The CK505's 100MHz SRC clock group consists of DPL_REFSSCLKINP and DPL_REFSSCLKINN. The 100MHz clock group is used by DisplayPort for SSC solution. For platforms that will not use integrated graphics or DisplayPort, the DPL_REFSSCLKINN/DPL_REFSSCLKINP outputs should be configured as 100 MHz SRC outputs or disabled during CK505 initialization. The DPL_REFSSCLKINN/ DPL_REFSSCLKINP inputs to the MCH should be terminated by routing DPL_REFSSCLKINP to 1.1V through a 10kΩ resistor and routing DPL_REFSSCLKINN directly to GND.

Please refer to SRC routing guidelines for routing DPL_REFSSCLKINN and DPL_REFSSCLKINP.

MICRO-START INT'L CO.,LTD.

Title: Eagle - MSIC		
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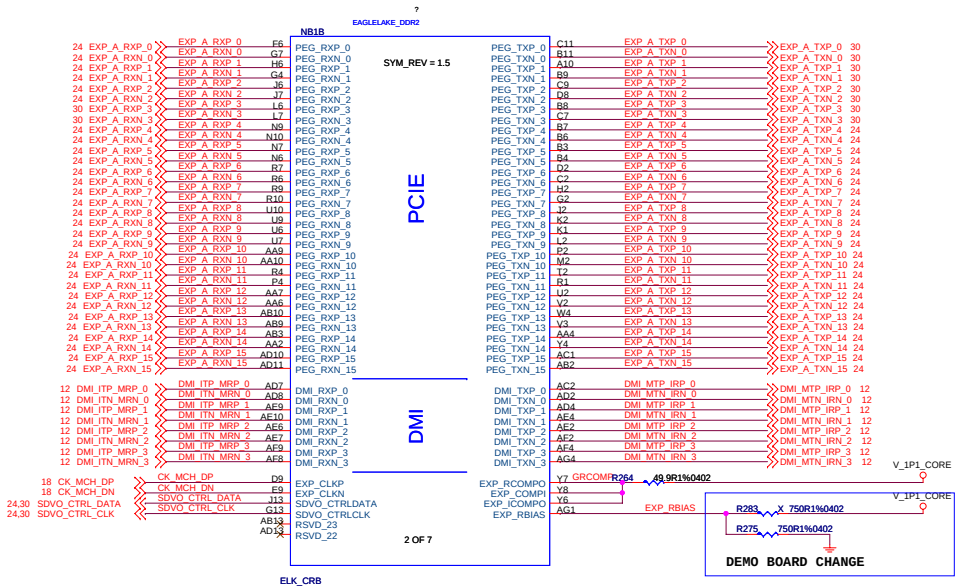

Primary _PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot

MSI MICRO-STAR INT'L CO.,LTD.

Title: Eagle - PCIE

Size	Document Number	Rev
C	MS-7524M1	0A

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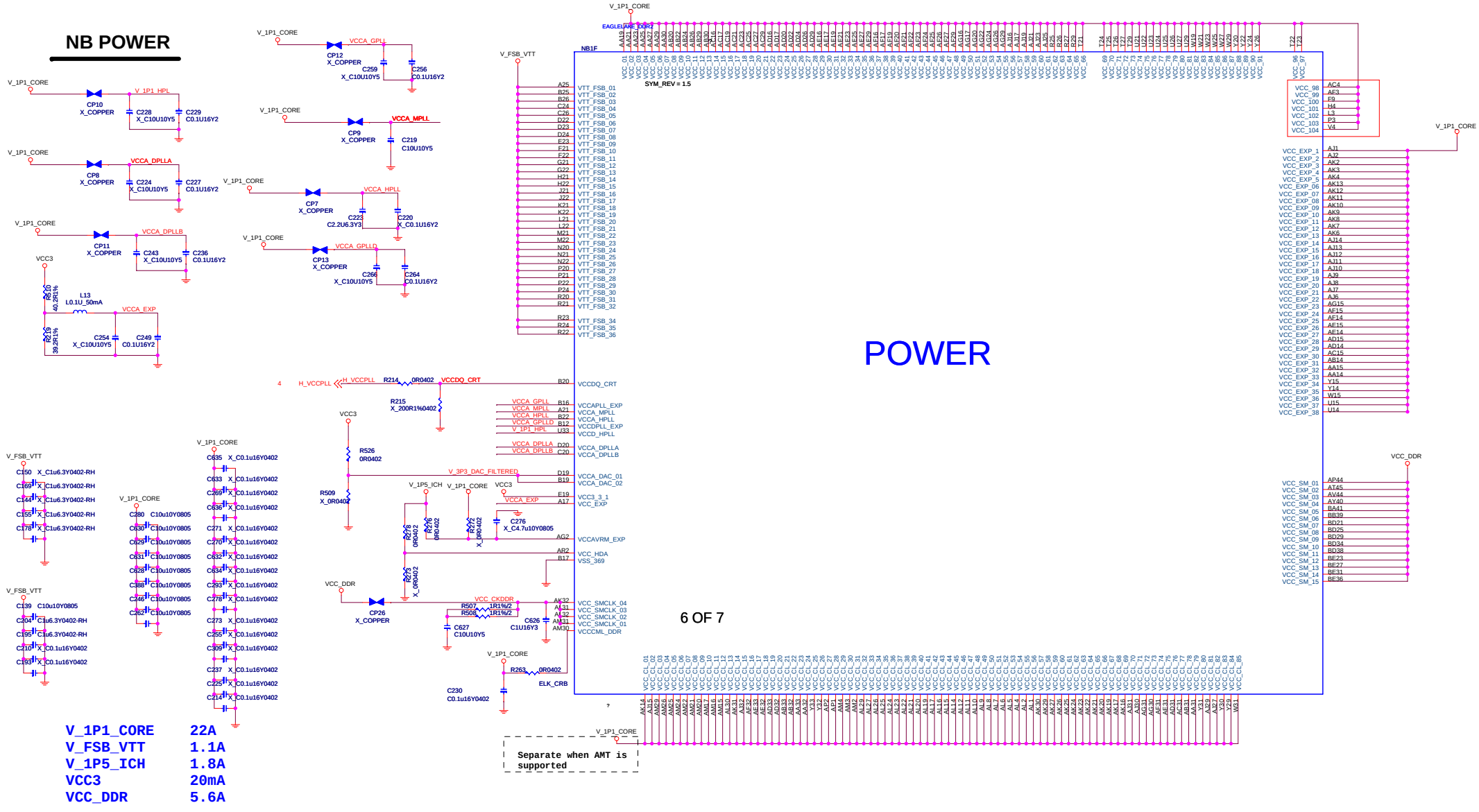
NB POWER



V_1P1_CORE	22A
V_FSB_VTT	1.1A
V_1P5_ICH	1.8A
VCC3	20mA
VCC_DDR	5.6A

Title	Eagle - Power
Size: Custom	Document Number: MS-7524M1
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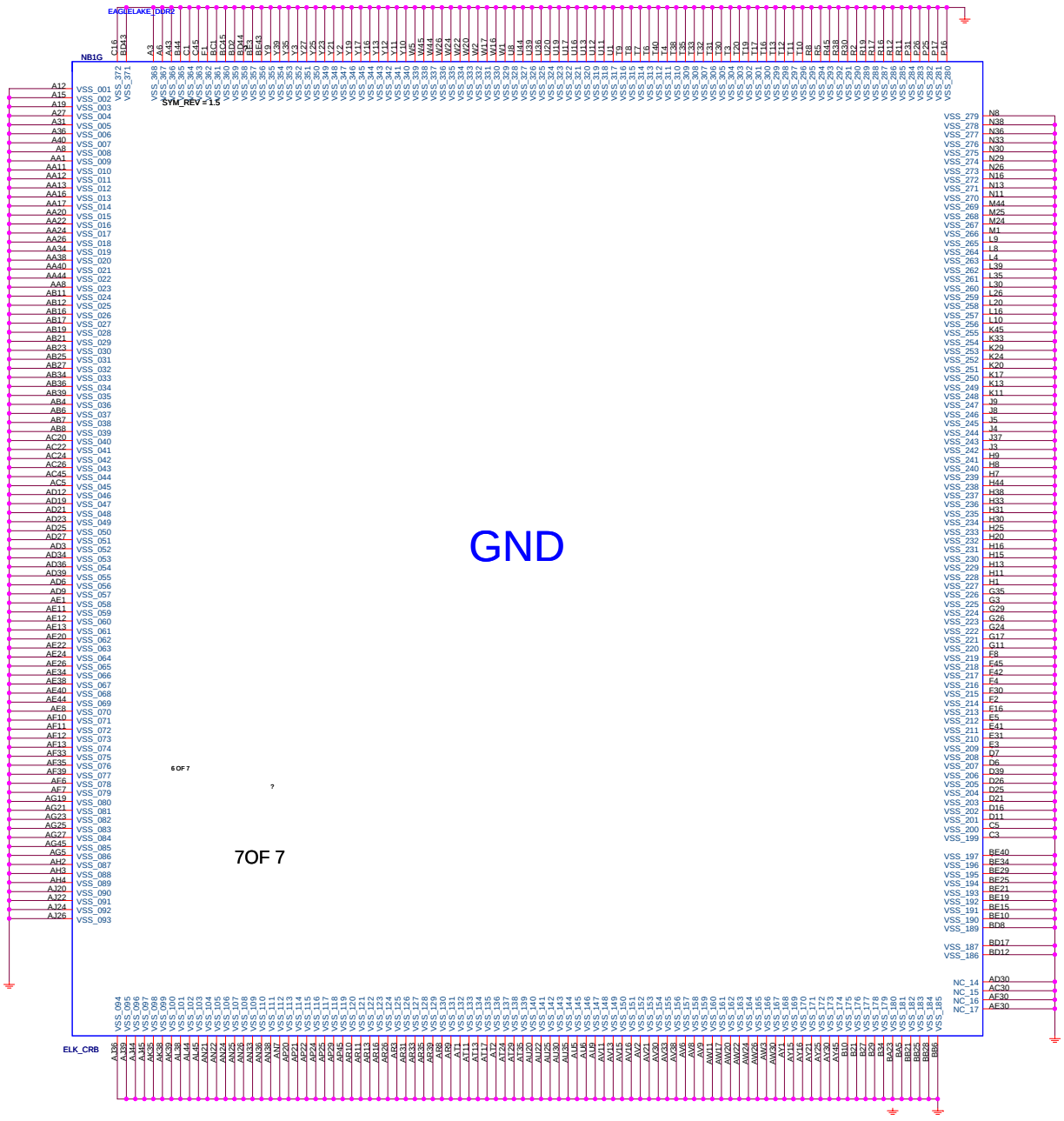
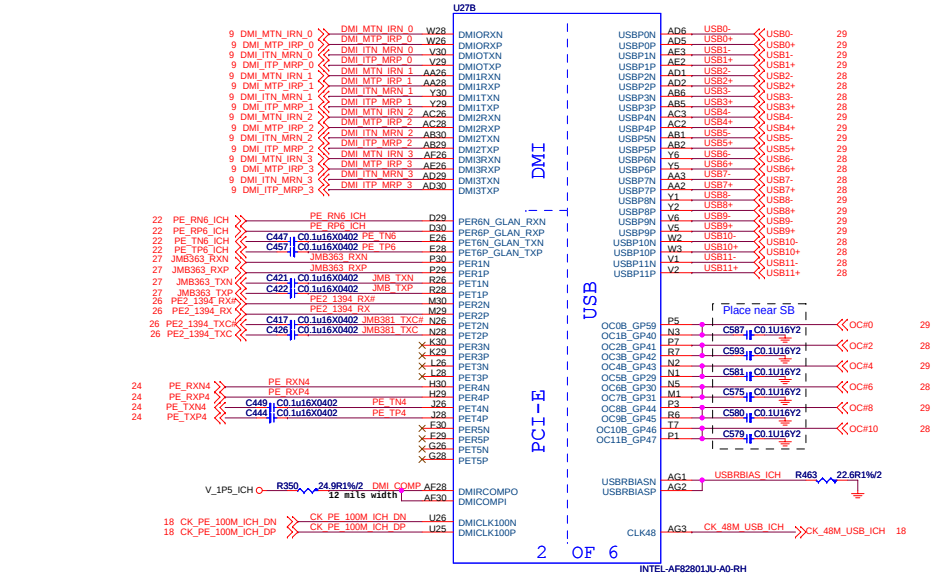
MICRO-START INT'L CO.,LTD.



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Eagle - GND		
Size C	Document Number MS-7524M1		Rev 0A
Date: Friday, March 14, 2008	Sheet 11 of 42		



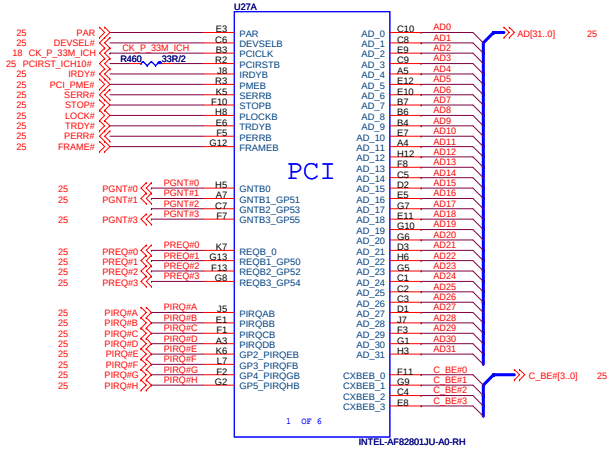
SB STRAPPING RESISTOR

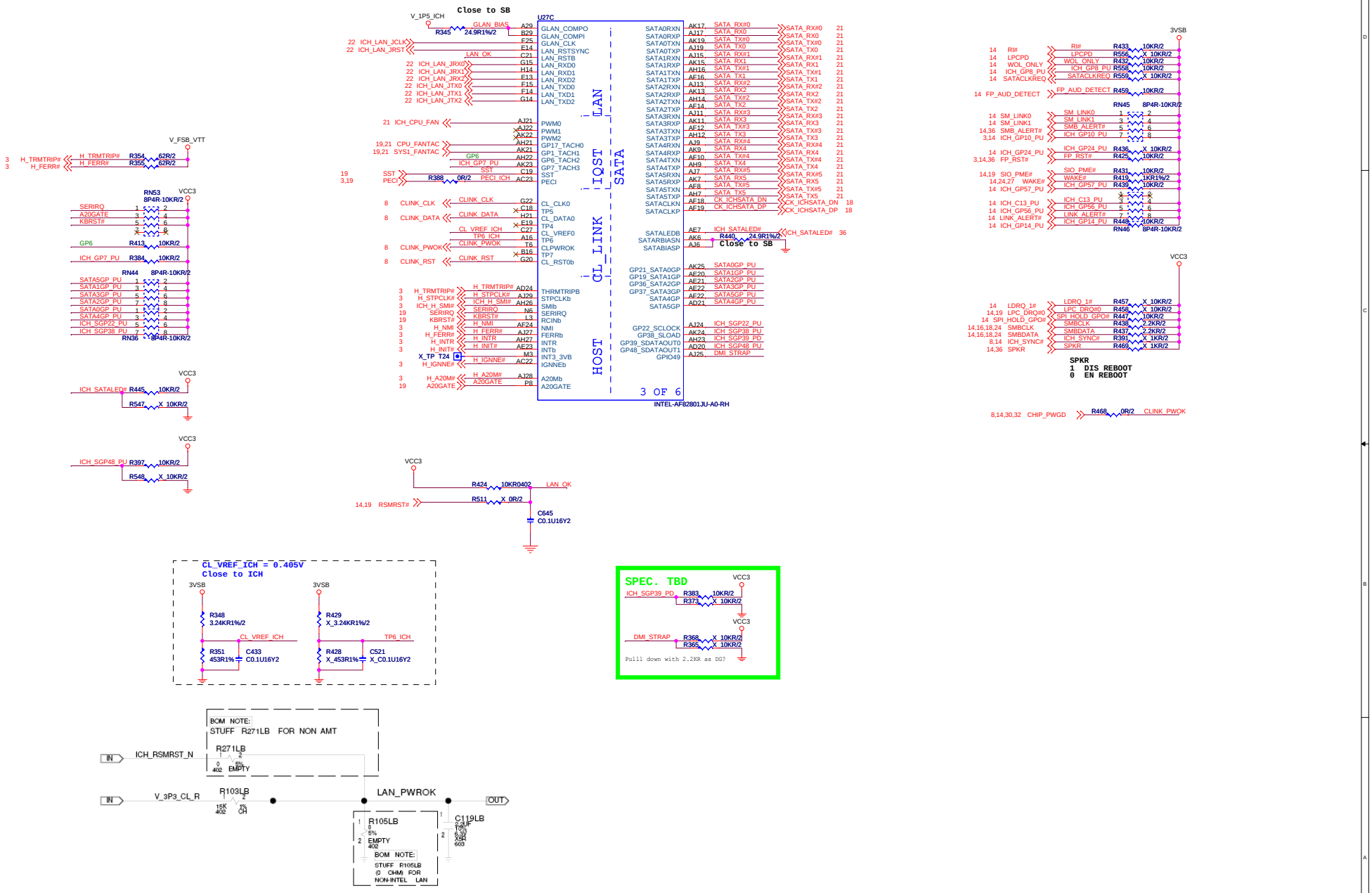
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

PGNT#[3:0]Internal Pull-up

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X





MICRO-START INT'L CO.,LTD.

Title: ICH10 - Host, SATA

Size	Document Number	Rev
C	MS-7524M1	0A

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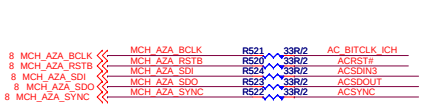
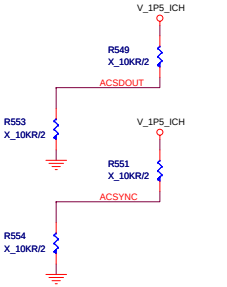
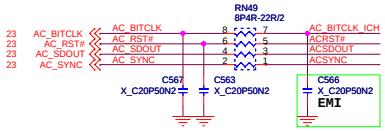


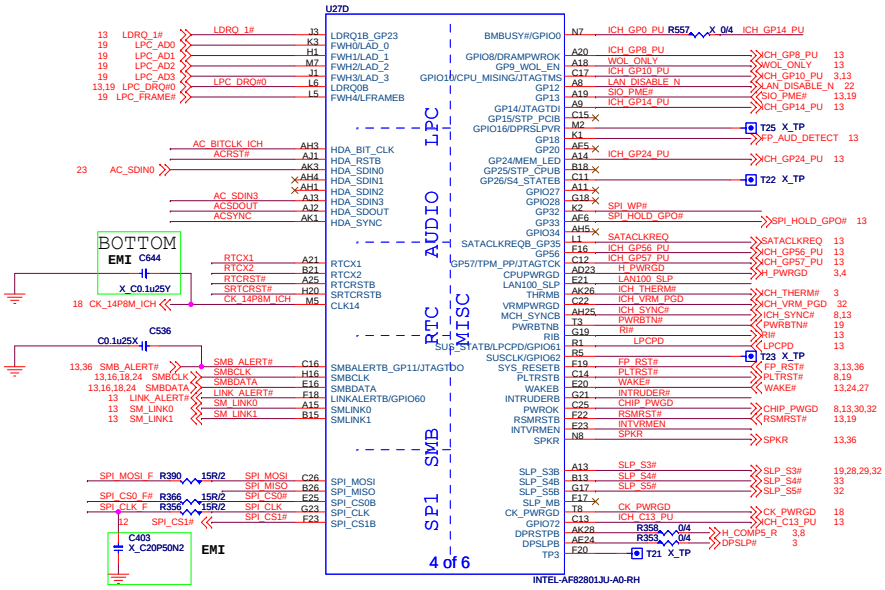


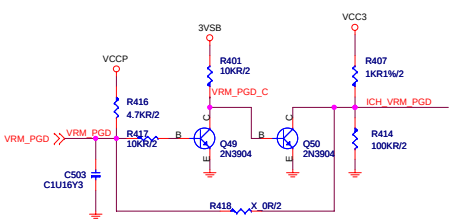
RPC—Root Port Configuration Register

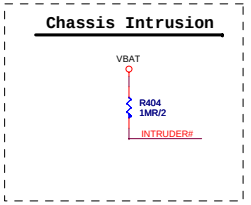
Offset Address: 0224–0227h Attribute: R/W, RO
Default Value: 0000000yh (y = 00xxb) Size: 32-bit

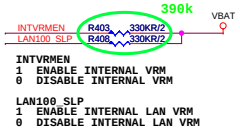
1:0	**Port Configuration (PC)** — RO. This controls how the PCI bridges are organized in various modes of operation for Ports 1-4. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. Consumer Only: These bits represent the strap values of HDA_SDOUT (bit 1) and HDA_SYNC (bit 0) when TP[3] is not pulled low at the rising edge of PWROK. Corporate Only: These bits are set by the PCIEPCS1[1:0] soft strap. 11 = 1 x4, Port 1 (x4) 10 = Reserved 01 = Reserved 00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1) and Port 4 (x1) These bits live in the resume well and are only reset by RSMRST#.







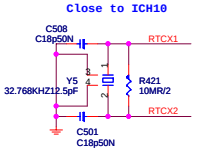


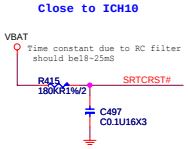


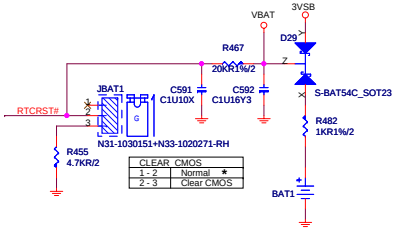
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM

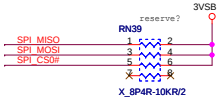
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM

RTC Block

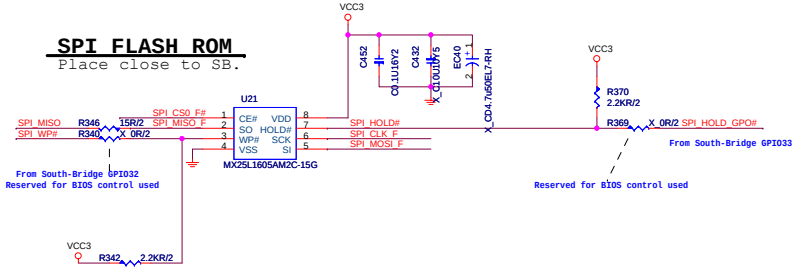




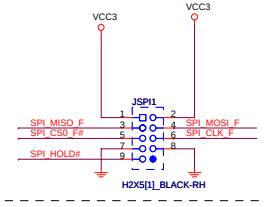


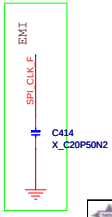


SPI FLASH ROM
Place close to SB.



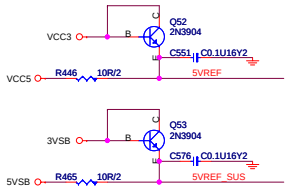
SPI DEBUG PROT
Close to SPI ROM





MSI MICRO-START INT'L CO.,LTD.
Title: ICH10 - RTC, MSIC
Size: C | Document Number: MS-7524M1 | Rev: 0A
Date: Wednesday, April 02, 2008 | Sheet 14 of 42

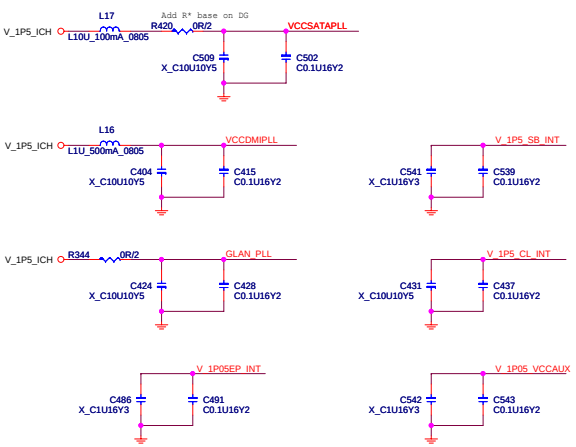
5VREF & 5VREF_SUS Sequencing Circuit



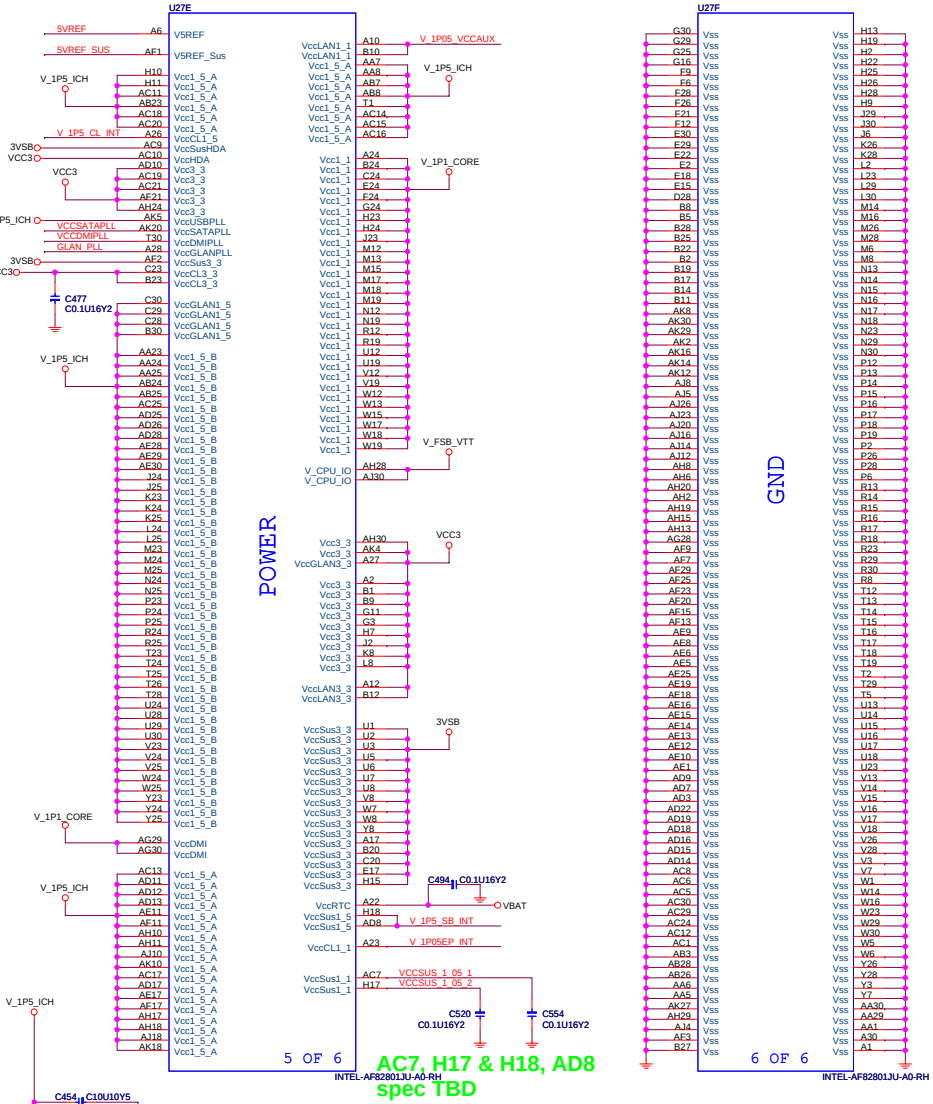
V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.

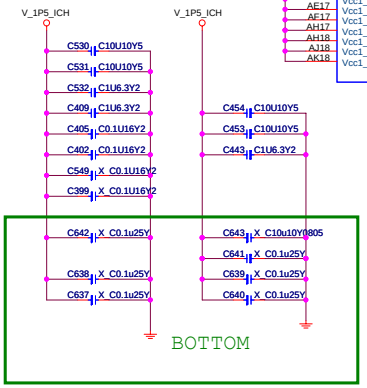
Symbol	Parameter	Min	Nom	Max	Unit
Vcc1_1 (Consumer Only)	Internal Logic Voltage	0.998	1.1	1.155	V
Vcc1_1 (Corporate Only)	Internal Logic Voltage	1.045	1.1	1.155	V

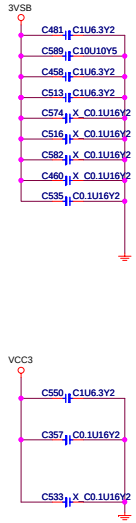
SB POWER



Power Plane	Maximum Power Consumption			
Symbol	S0	S3	S4/S5	G3
VccLAN1_05[2, 5]	Powered by Vcc1_05 in S0	Powered by VccLAN3_3 in S3	Powered by VccLAN3_3 in S4/ S5	N/A
VccCL3_3	19 mA	73 mA	73 mA	N/A
VccCL1_5[2]	Powered by Vcc1_5_A in S0	Powered by VccCL3_3 in S3	Powered by VccCL3_3 in S4/S5	N/A
VccCL1_12	Powered by Vcc1_1 in S0	Powered by VccCL3_3 in S3	Powered by VccCL3_3 in S4/S5	N/A
Vcc1_5_A	1.644 A	N/A	N/A	N/A
Vcc1_5_B	646 mA	N/A	N/A	N/A
VccSus1_52	Powered by Vcc1_5_A in S0	Powered by VccSus3_3 in S3	Powered by VccSus3_3 in S4/S5	N/A
Vcc1_1	1.634 A	N/A	N/A	N/A
VccSus1_12	Powered by Vcc1_1 in S0	Powered by VccSus3_3 in S3	Powered by VccSus3_3 in S4/S5	N/A
VccRTC[3, 4]	N/A	N/A	N/A	6 µA
VccDMI[7]	50 mA	N/A	N/A	N/A
V_CPU_IO	2 mA	N/A	N/A	N/A
VccGLANPLL	23 mA	N/A	N/A	N/A
VccUSBPLL	11 mA	N/A	N/A	N/A
VccDMIPLL[7]	23 mA	N/A	N/A	N/A
VccSATAPLL	47 mA	N/A	N/A	N/A





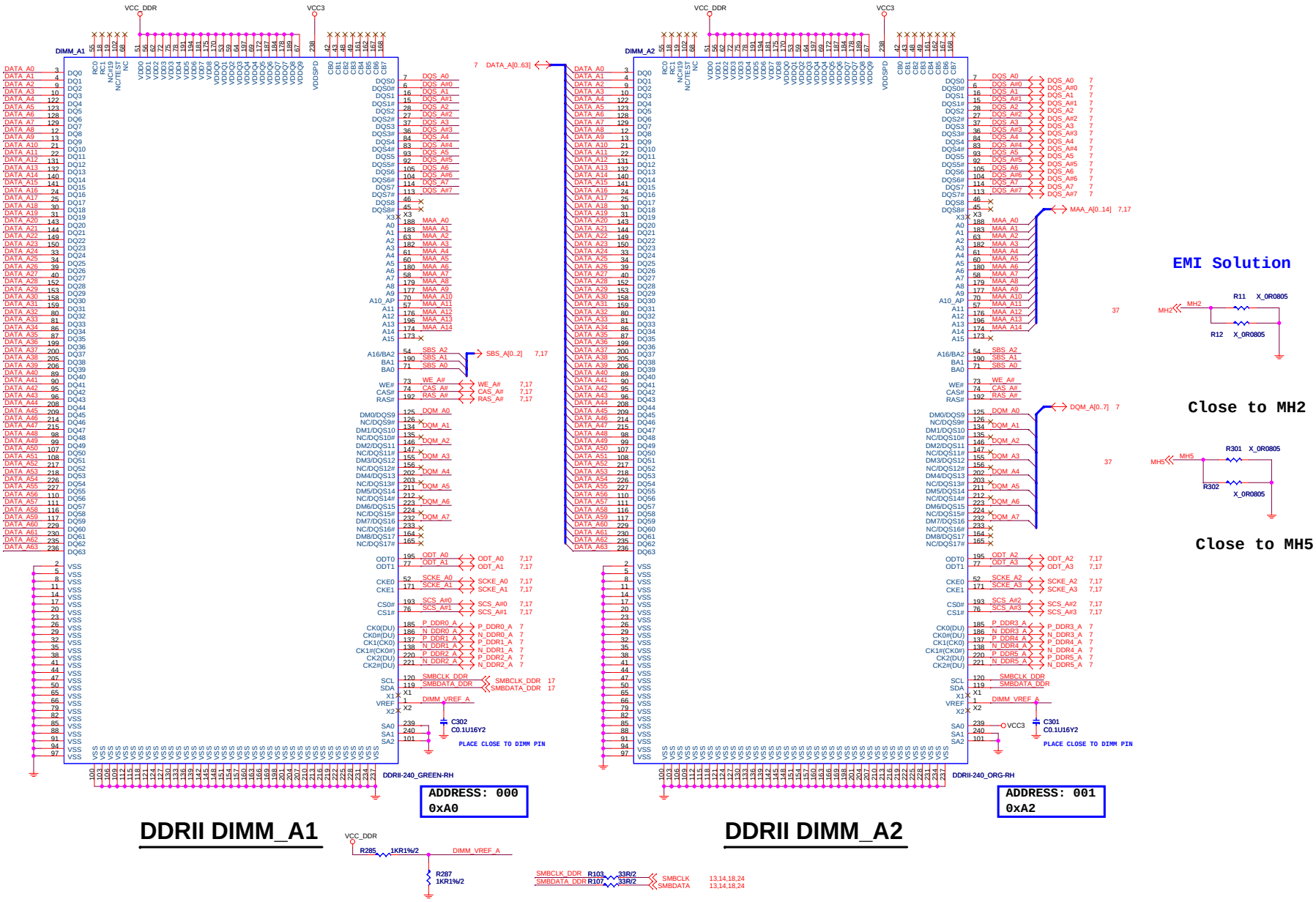


MSI MICRO-START INT'L CO.,LTD.

Title: ICH10 - Power, GND

Size: C | Document Number: MS-7524M1 | Rev: 0A

Date: Thursday, March 27, 2008 | Sheet 15 of 42

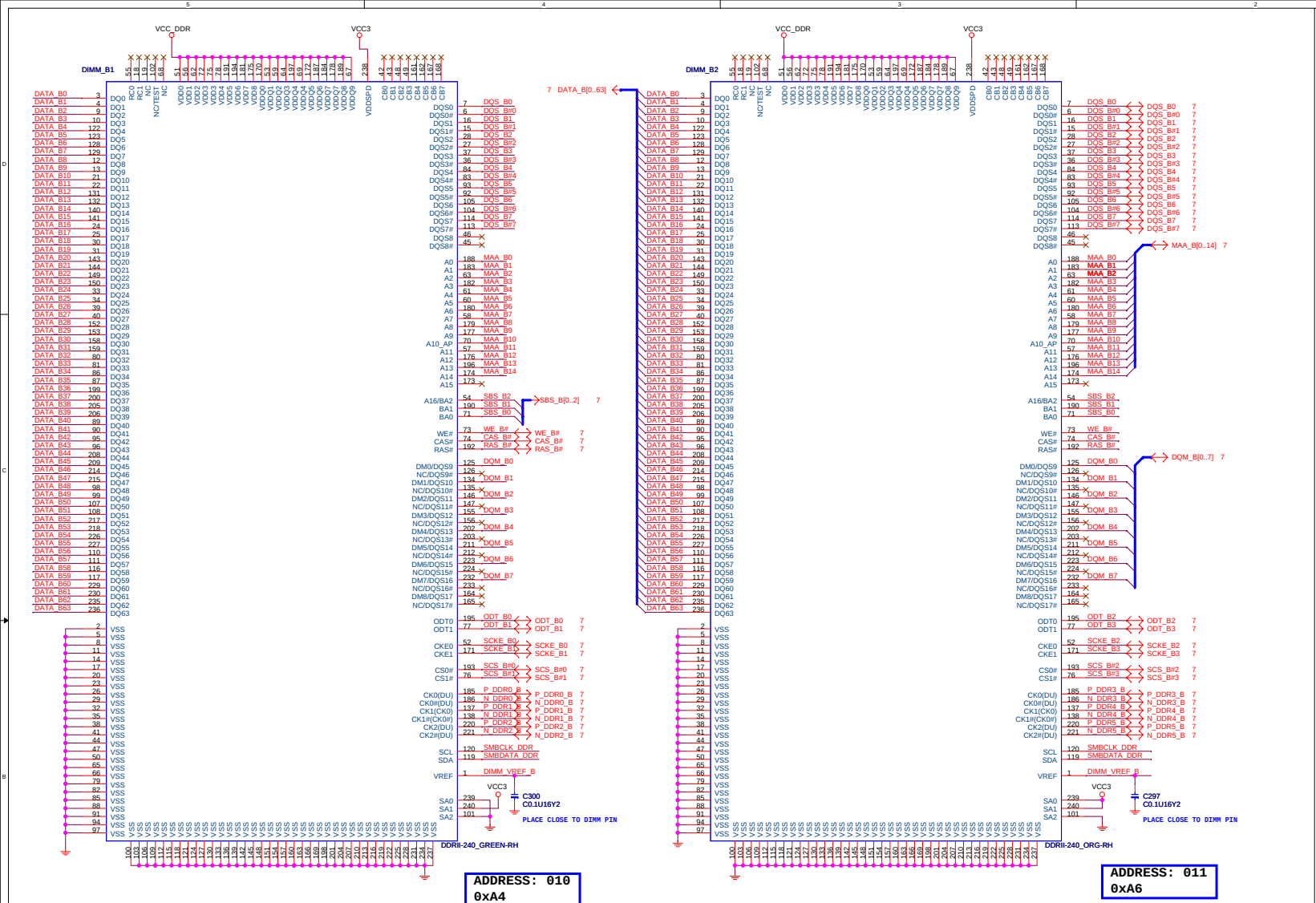


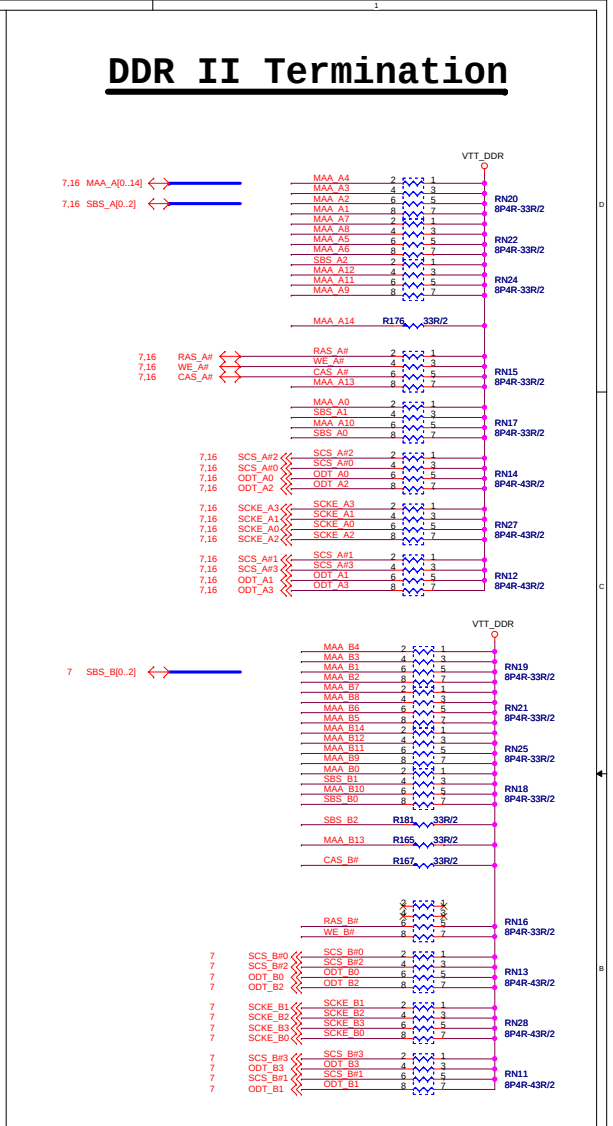
MSI MICRO-STAR INT'L CO.,LTD.

Title: DDR2 Channel 1

Size	Document Number	Rev
C	MS-7524M1	0A

Date: Wednesday, April 02, 2008 Sheet 16 of 42





MICRO-START INT'L CO.,LTD.

Title: DDR2 Channel 2 / Termination

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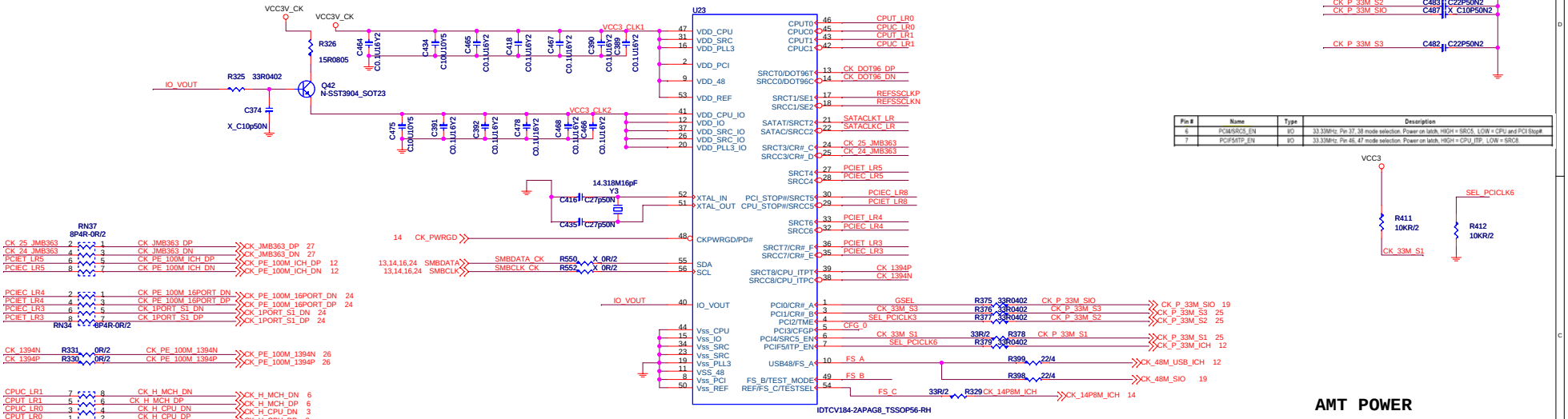
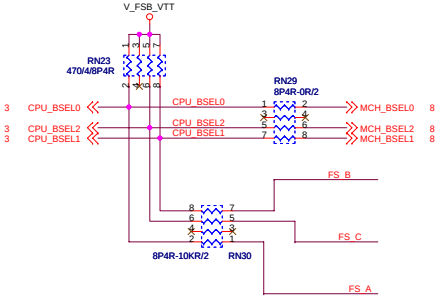
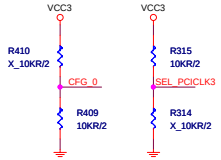
Symbol	Description	Conditions	Min	Typ	Max	Unit
Idd_3.3V	Operating Supply Current, default configuration				250	mA
Idd_IO_3.3V	Differential I/O current, all output enabled				80	mA







CFGP, TME (pin5, pin4)	CFG1, CFG0 Byte11 bit[7:6]
Low, 0	0, 0
Low, 1	0, 0
Mid, 0	0, 1
Mid, 1	0, 1
High, 0	1, 0
High, 1	1, 1

CFG Configuration Table 2

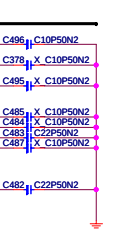
CFG[1: 0]	CPU	SATA (pin21, 22)	PCI	Pin17/ 18	SRC	48/96
00	PLL1(1)	PLL4 SRC(1)	PLL4 (from SRC PLL)(1)	CFB table (default SRC)	PLL4(1)	PLL2(3)
01	PLL1(1)	PLL3(1)	PLL3(1)	CFB table (default SRC)	PLL4(1)	PLL2(3)
10	PLL1(2)	PLL3(1)	PLL3(1)	CFB table (default SRC)	PLL4(1)	PLL2(3)
11	PLL1(2)	PLL2 (CV184-1)(3) PLL4 (CV184-2)(1)	PLL4(1)	Pin17 = 25MHz, PLL2 Pin18 = 1394A, PLL3(3)	PLL4(1)	PLL2(3)

Note:
1. SSC 0.5% down spread
2. SSC 0.5% center spread
3. No SSC

CFB TABLE (PIN 17-18)

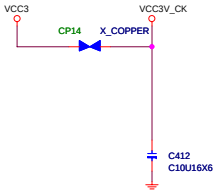
CFB[3,2,1,0]	Pin17, 18	Comments
0000	SRC (PLL4)	SATA/PCI from PLL3 or PLL4 (see CFG table)
0001	SRC (PLL4)	default, SATA/PCI from PLL3 or PLL4 (see CFG table)
0010	100MHz 0.5% SSC (PLL3)	From PLL3 , SATA/PCI from PLL4
0011	100MHz 1.0% SSC (PLL3)	From PLL3 , SATA/PCI from PLL4
0100	100MHz 1.5% SSC (PLL3)	From PLL3 , SATA/PCI from PLL4
0101	100MHz 2.0% SSC (PLL3)	From PLL3 , SATA/PCI from PLL4
110	100MHz 2.5% SSC (PLL3)	From PLL3 , SATA/PCI from PLL4
0111	**Reserved**	From PLL3 , SATA/PCI from PLL4
1000	1394A 3.3V, SSC off Byte4 bit0 lose control	From PLL3 , SATA/PCI from PLL4
1001	1394A&B 3.3V, SSC off Byte4 bit0 lose control	From PLL3, pin17 = 1394A, pin18 = 1394B, SATA/PCI from PLL4
1010	1394B 3.3V, SSC off Byte4 bit0 lose control	From PLL3 , SATA/PCI from PLL4
1011	27MHz, 3.3V, Byte4 bit0 control the SSC enable, Byte1 bit5 control the down/center	From PLL3 , SATA/PCI from PLL4
1100	25MHz 3.3V, SSC off Byte4 bit0 lose control	From PLL3 , SATA/PCI from PLL4
1101	Pin17 = 25MHz, PLL2 Pin18 = 1394A, PLL3 Both no SSC	25MHz from PLL2 1394 from PLL3, SATA/PCI from PLL4
1110	Reserved	Reserved
1111	Reserved	Reserved

FS_C	FS_B	FS_A	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT_96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					



Pin #	Name	Type	Description
6	PCI4/SRC5_EN	I/O	33.33MHz. Pin 37, 38 mode selection. Power on latch, HIGH = SRC5, LOW = CPU and PCI Stop#
7	PCIF5/ITP_EN	I/O	33.33MHz. Pin 46, 47 mode selection. Power on latch, HIGH = CPU_ITP, LOW = SRC8.

AMT POWER



MSI
MICRO-START INT'L CO.,LTD.

Title: IDTCV184

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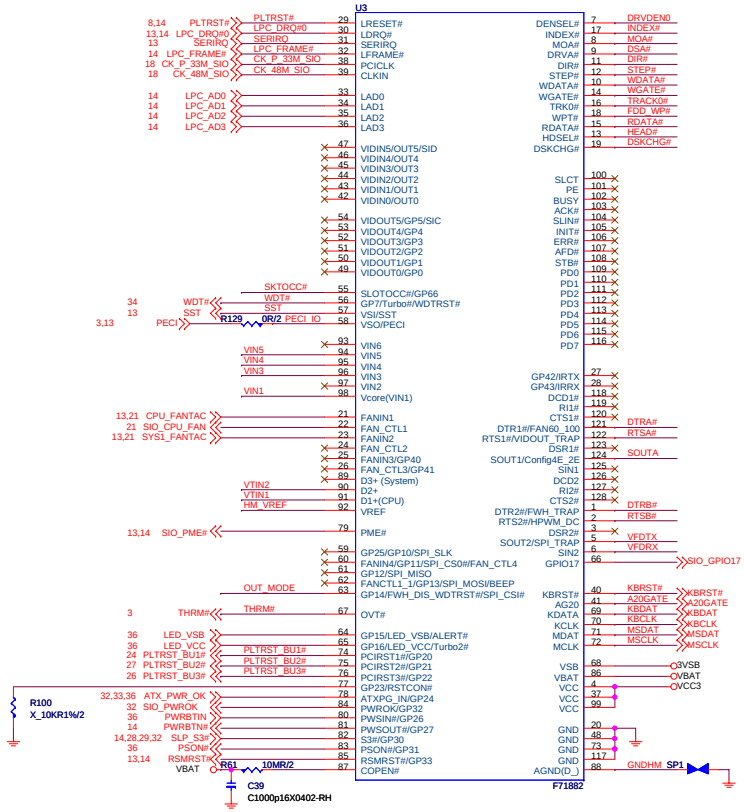


PCI Reset and PWROK Signals

The F71882FG supports 3 output buffers for 3 reset signals. If the register RSTCON_EN is set to 1, the pin RSTCON# will infect PCIRST1# ~ PCIRST3# outcome. Then, the result of PCIRST# outcome will be affected by conditions as below:

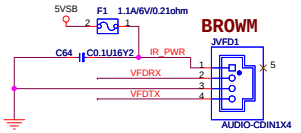
PCIRST1# → Output buffer of RSTCON# and LRESET#.
PCIRST2# → Output buffer of RSTCON# and LRESET#.
PCIRST3# → Output buffer of RSTCON# and LRESET#.

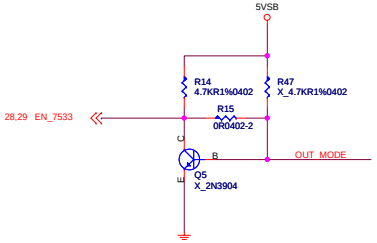
So far as the PWROK issue is as the figure above. PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register. (100ms ~ 400ms)

In the figure, the RSTCON# will be implemented by register RSTCON_EN. If RSTCON_EN be set to 0, the RSTCON# pin will affect PWROK outputs(Default). If RSTCON_EN be set to 1, the RSTCON# pin will affect PCIRST outputs.

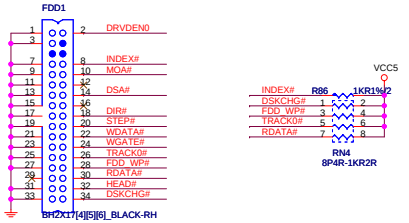
Front LCD (SERIAL PORT 2)

Parameter	Typ	Unit
Main Supply Average Current	5	mA
Main Supply Standby Current	2.5	mA
Standby Supply Average Current	1.0	mA
Battery Supply Current	0.24	uA

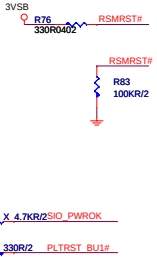




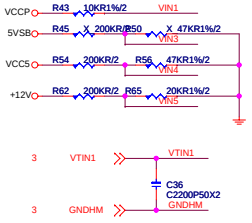
FLOPPY CONNECTOR



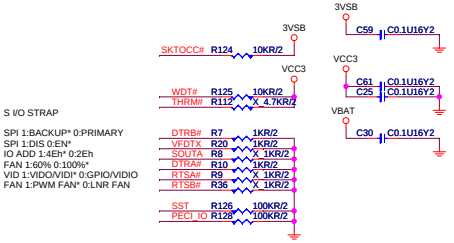
Pin No.	Pin Name	Type	PWR	Description
84	PWROK	OD_{12}	VSB	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.



Thermal Resistor



LPC I/O STRAPPING RESISTOR



Title: F71882
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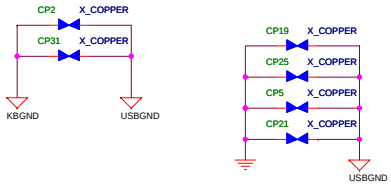
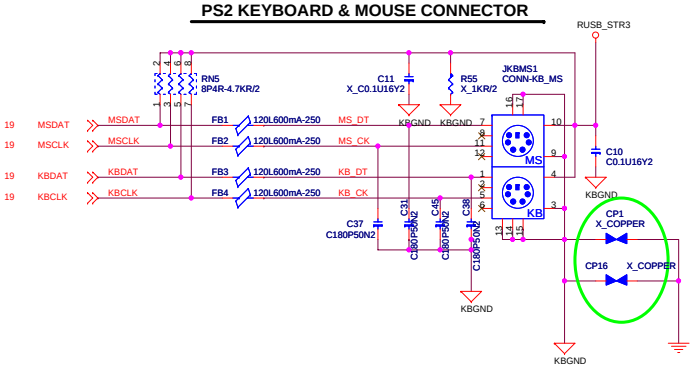
EMI Solution





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Title: PS2 Keyboard & Mouse		
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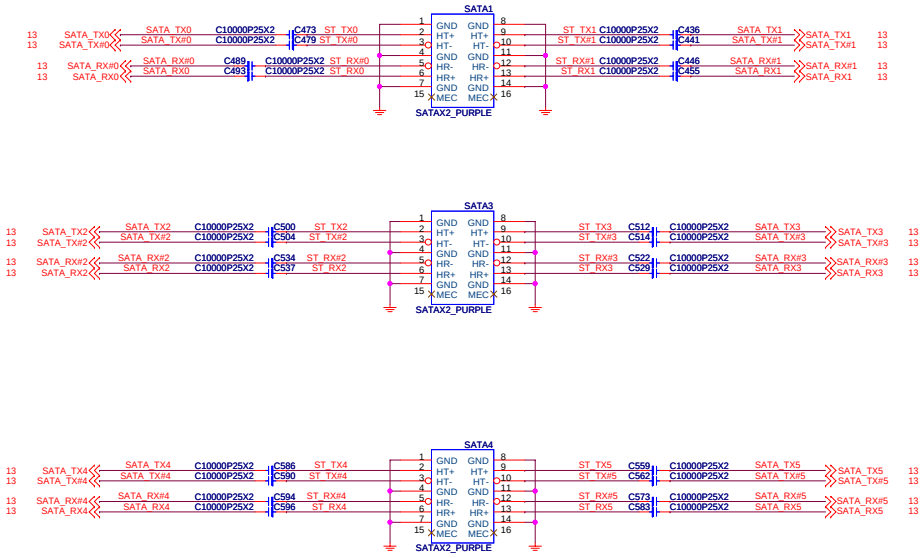
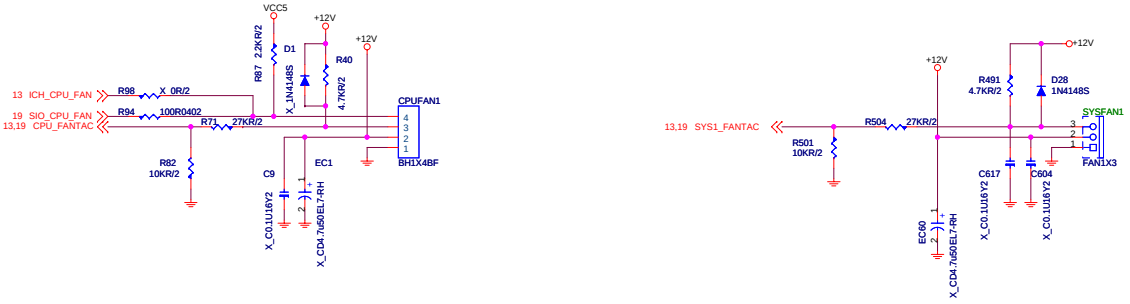


FAN-COUNTROL CIRCUIT



Modify System FAN circuit & Remove PWR_FAN
for spec need 3pin DC Smart FAN 07.3.30 by Robile

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Title: SATA / FAN Control

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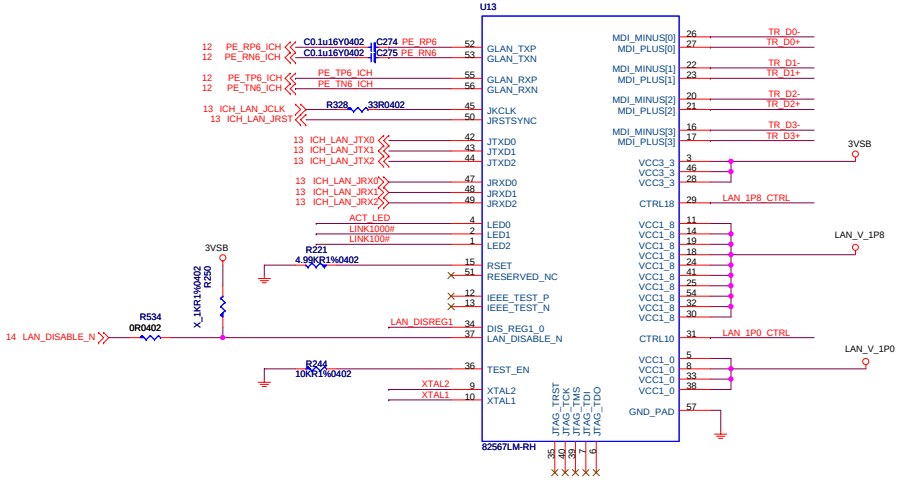
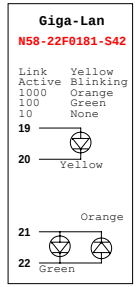
Maximum current of 1.8 V is less then 270mA, Maximum current of 1.0 V is less then 139mA.

For proper and safe operation, the power supplies must follow the following rule:

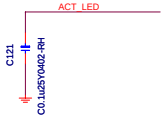
VDDO (3.3V) ≥ AVDD (1.8) ≥ DVDD (1.05V)

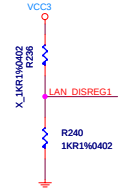
This means that VDDO must start ramping before AVDD and DVDD, but DVDD may reach its nominal operating range before AVDD and VDDO.

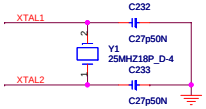


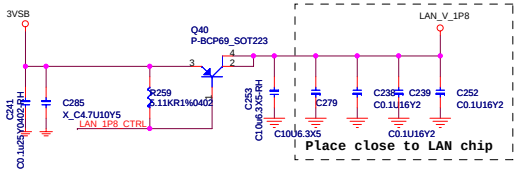


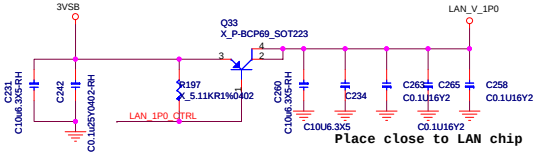
EMI Solution

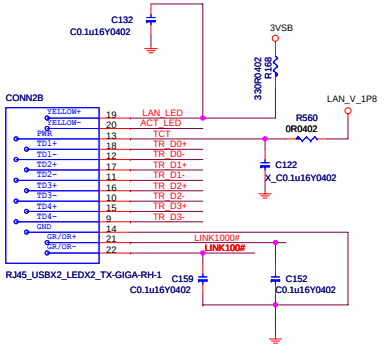












MSI MICRO-STAR INT'L CO.,LTD.		
Title: Intel82567		
Size: C	Document Number: MS-7524M1	Rev: 0A
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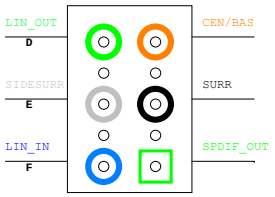
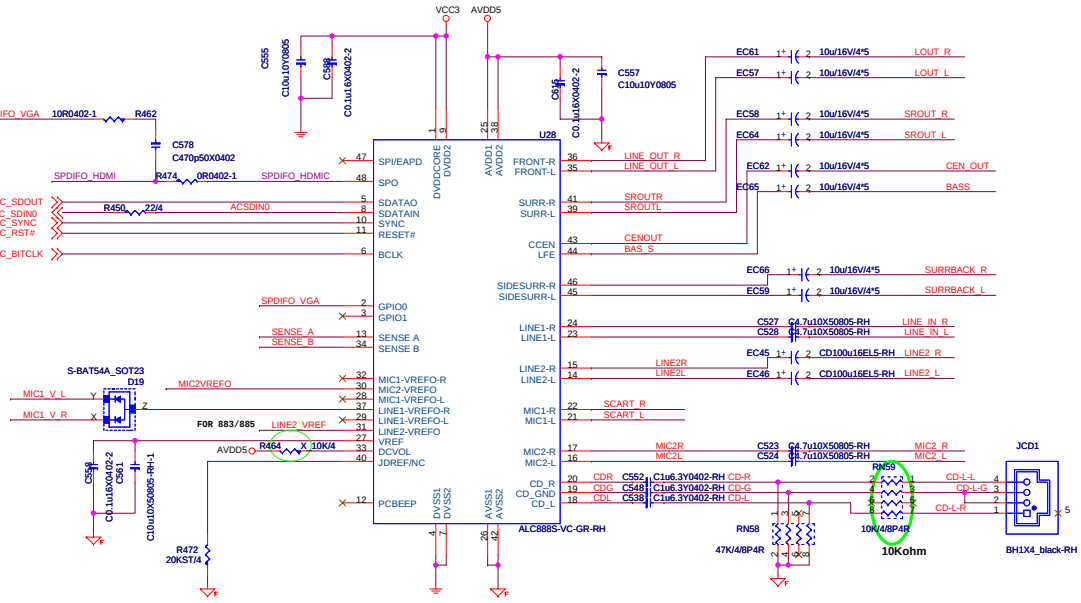
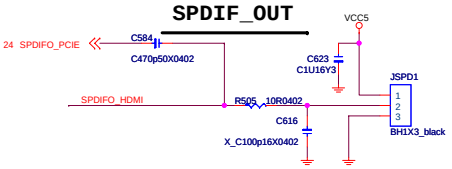
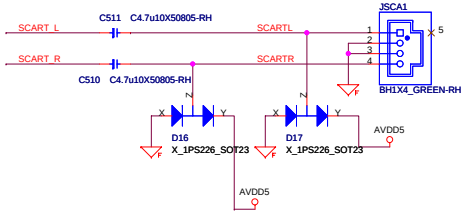
Description	D0
1~12 DVDD	35.5
13~48 AVDD	50.1

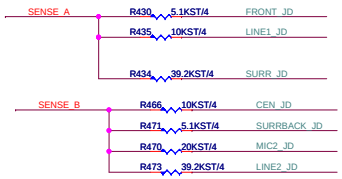
	ALC888	ALC888S
Del	c573	R938
	R441	

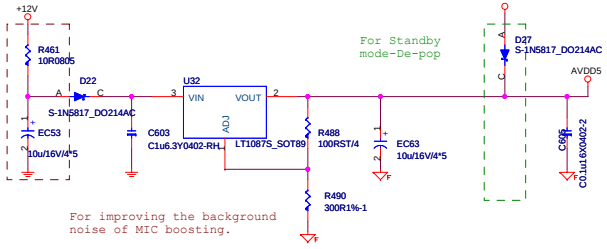


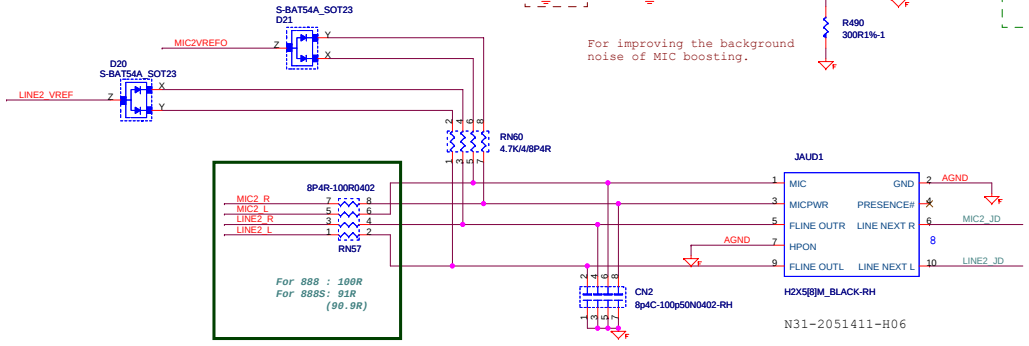


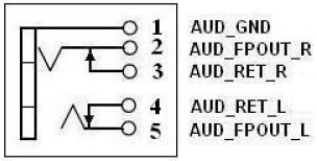


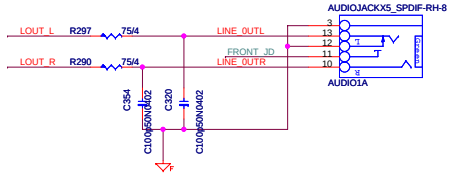


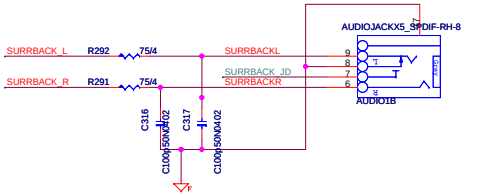


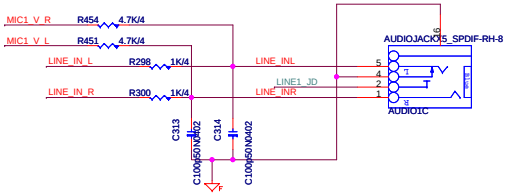


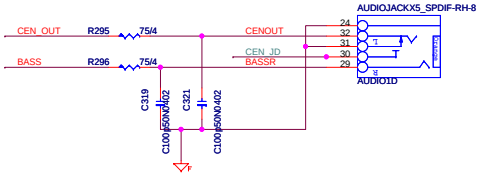


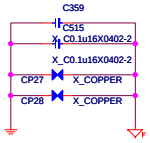


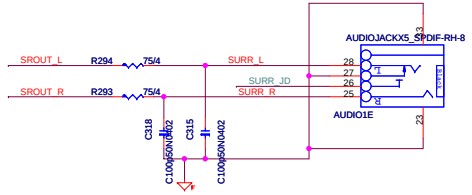


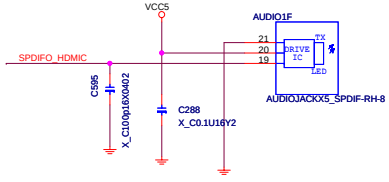












N31-2051411-H06

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Title: ALC888

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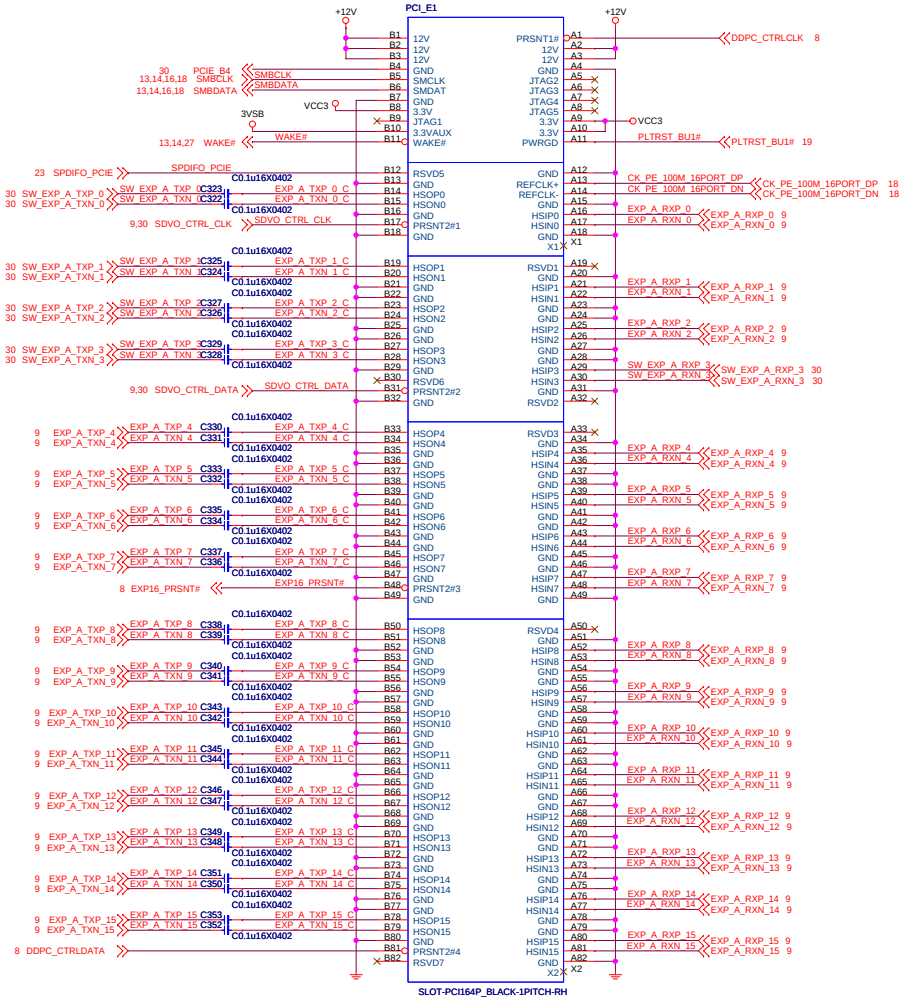
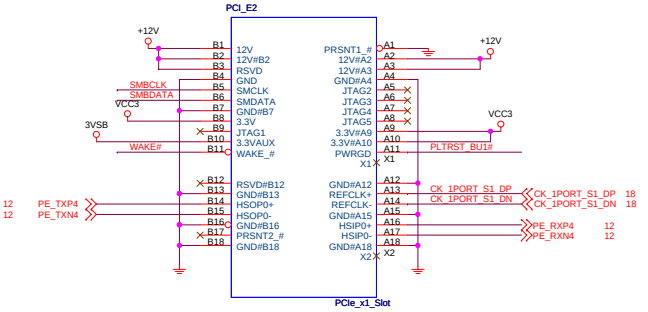
PCI_Express X16 Slot

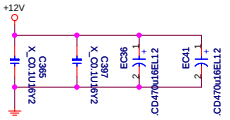


+12V 5.5A VCC3 3A

PCI_Express X4 Slot
(Share with PCI_E x1 Slots)



+12V 0.5A VCC3 3A



MSI MICRO-STAR INT'L CO.,LTD.		
Title: PCIE x16 & x1		
Size: C	Document Number: MS-7524M1	Rev: 0A
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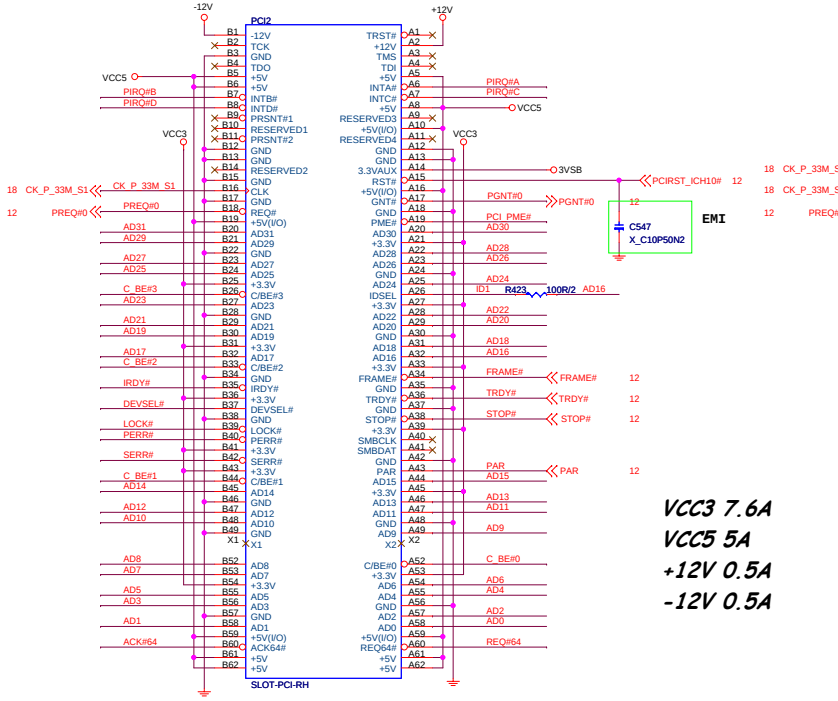
PCI SLOT 2 (PCI VER: 2.2 COMPLY)

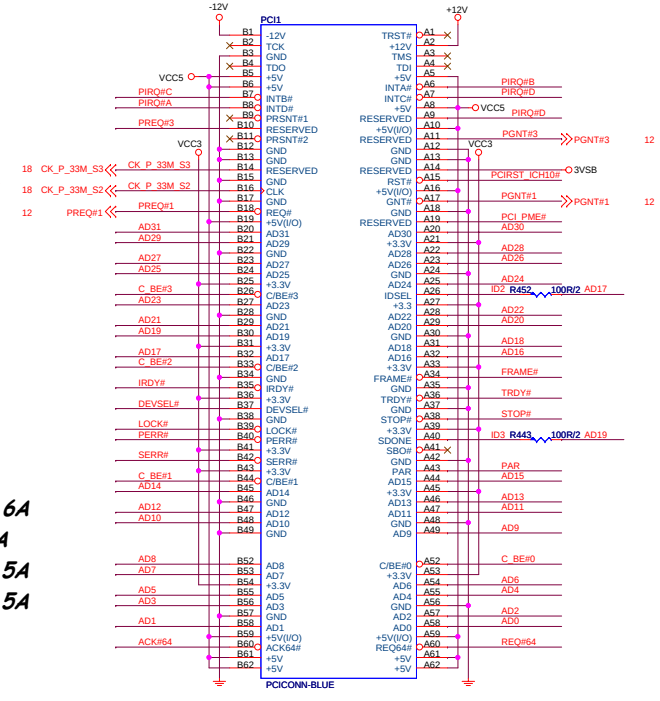


VCC3 7.6A
VCC5 5A
+12V 0.5A
-12V 0.5A

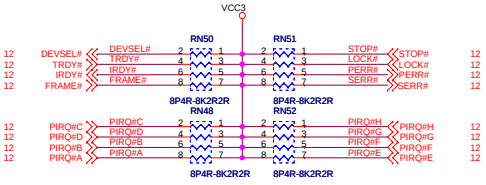
12 AD[31..0] AD[31..0]

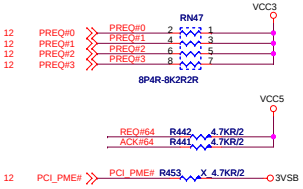
12 C_BE#[3..0] C_BE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

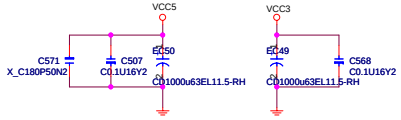


PCI PULL-UP / DOWN RESISTORS





PCI SLOT DECOUPLING CAPACITORS



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Title: PCI Slot 1 & 2		
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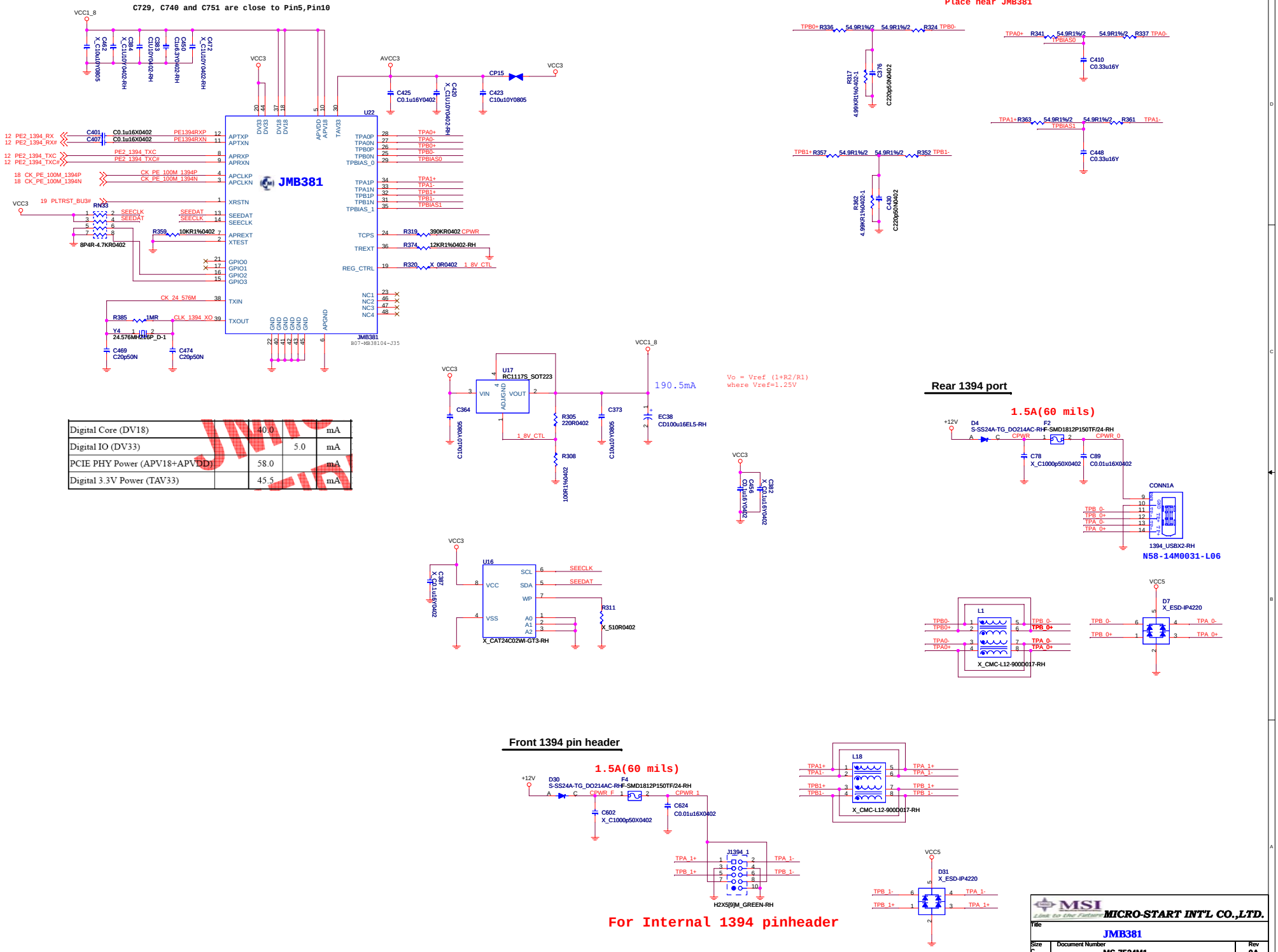
C729, C740 and C751 are close to Pin5,Pin10
Place near JMB381
JMB381
U22
APTXP
APTXN
APRXP
APRXN
APCLKP
APCLKN
XRSTN
SEEDAT
SEECLK
APREXT
XTEST
GPIO0
GPIO1
GPIO2
GPIO3
TXIN
TXOUT
TPA0P
TPA0N
TPB0P
TPB0N
TPBIAS_0
TPA1P
TPA1N
TPB1P
TPB1N
TPBIAS_1
TCPS
TREXT
REG_CTRL
NC1
NC2
NC3
NC4
JMB381
B07-MB3B104-J35
U17
RC1117S_SOT223
190.5mA
Vo = Vref (1+R2/R1)
where Vref=1.25V
U16
X_CAT24C02WI-GT3-RH
Rear 1394 port
1.5A(60 mils)
CONN1A
1394_USBX2-RH
N58-14M0031-L06
X_CMC-L12-900D017-RH
X_ESD-IP4220
Front 1394 pin header
1.5A(60 mils)
J1394_1
H2X5[9]M_GREEN-RH
For Internal 1394 pinheader
L18
D31
Digital Core (DV18) 140.0 mA
Digital IO (DV33) 5.0 mA
PCIE PHY Power (APV18+APVDD) 58.0 mA
Digital 3.3V Power (TAV33) 45.5 mA
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MICRO-START INT'L CO.,LTD.
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JMB381
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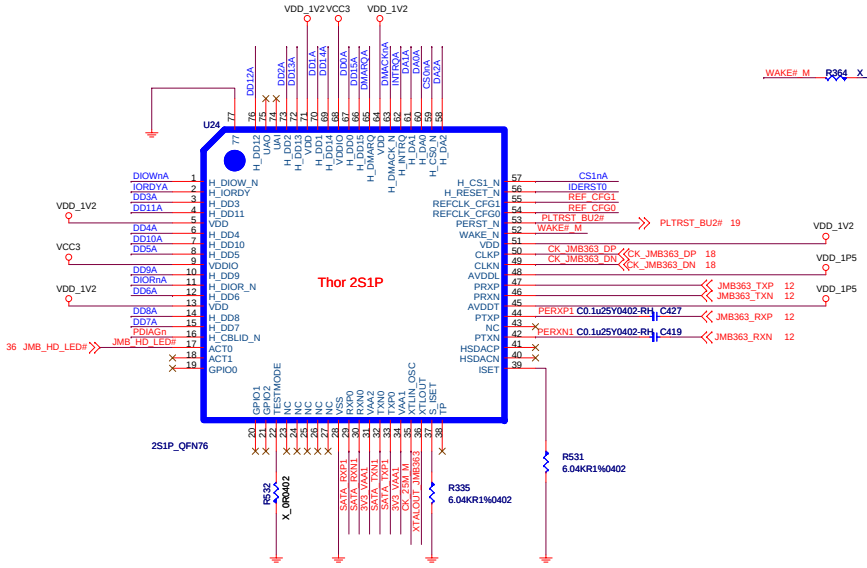
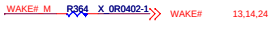
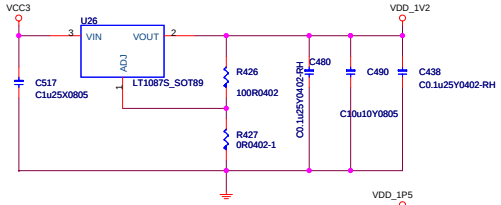
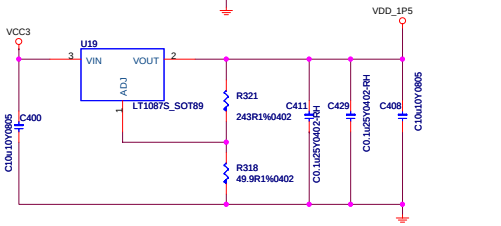
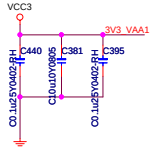


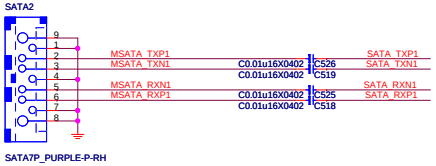


min 15mil. **361.3 mA**

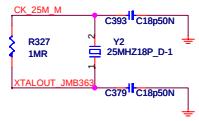


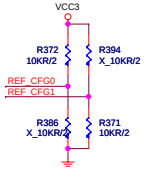




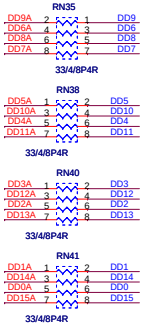


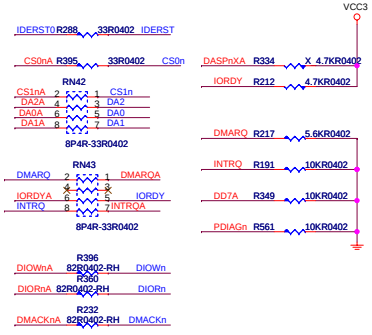
Parameter	Symbol	Min	Typ	Max	Units
Analog Power for PCI-E Phy (1.5V)	I_{AVDDT}/I_{AVDDL}		65		mA
Analog Power for Crystal Oscillator, PLL, PCI	I_{VAA1}		25		mA
Analog Power for SATA Phy	I_{VAA2}		75		mA
Digital Core Power	I_{VDD}		170		mA
Digital I/O Power	I_{VDDIO}		30		mA

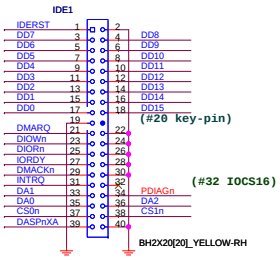




REF_CFG[1:0] =
00:20MHz
01:25MHz







if the length of JMB-363 to IDE connector more than 4inch, that must stuff dampping resistor.

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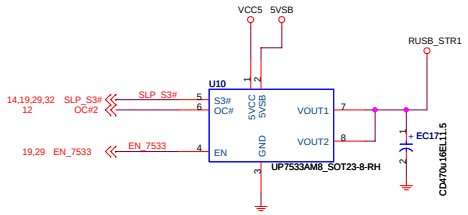
Rear USB Connector

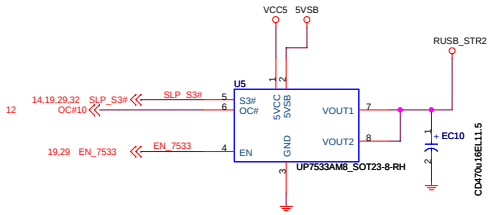
USB POWER FOR PORT 2,3

NEAR CONNECTOR



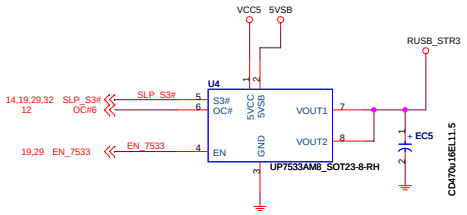
USB POWER FOR PORT 10,11

NEAR CONNECTOR

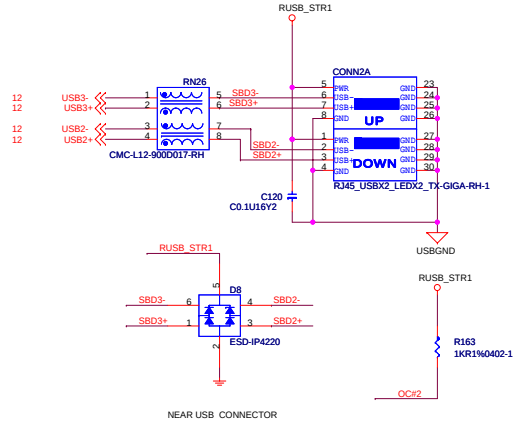


USB POWER FOR PORT 6,7

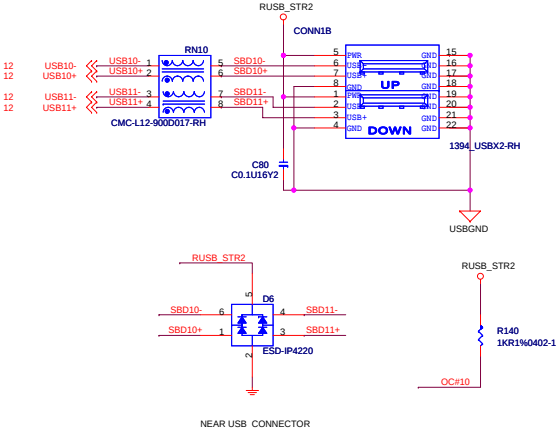
NEAR CONNECTOR



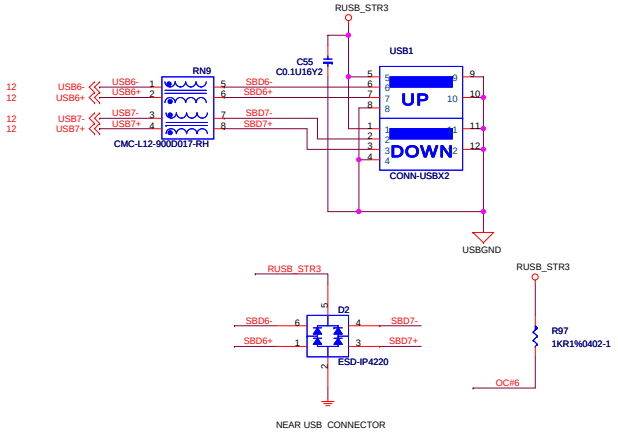
REAR USB PORT 2,3



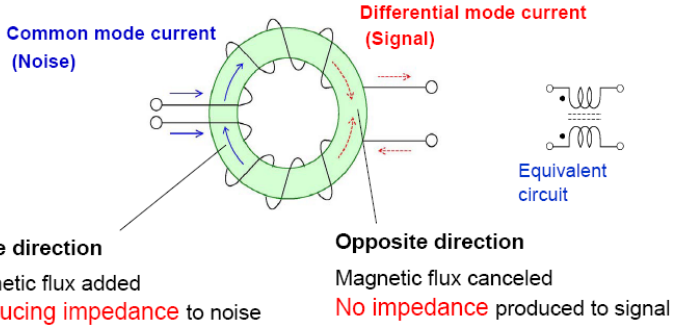
REAR USB PORT 10,11



REAR USB PORT 6,7



	S0/S1	S3	S4/S5
USB	500mA	500mA	500mA
PS2	300mA	300mA	300mA



MICRO-START INT'L CO.,LTD.

Title: Rear USB Connectors

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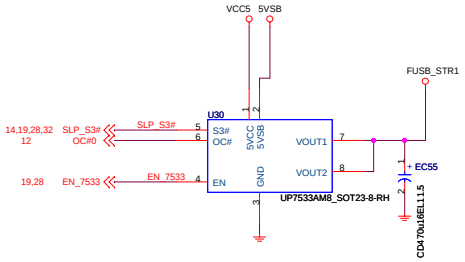
Front USB Connector

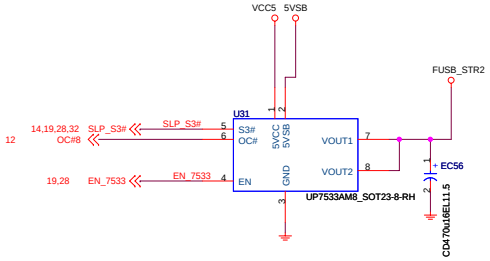
USB POWER FOR PORT 0,1

NEAR CONNECTOR



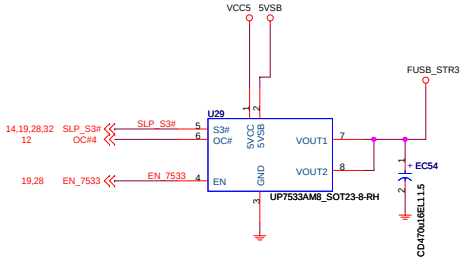
USB POWER FOR PORT 8,9

NEAR CONNECTOR

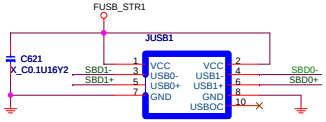


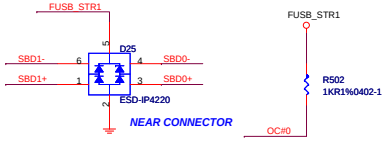
USB POWER FOR PORT 4,5

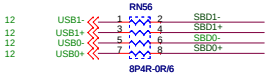
NEAR CONNECTOR



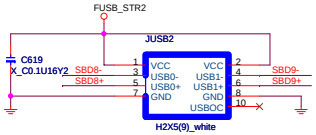
FRONT USB PORT 0,1

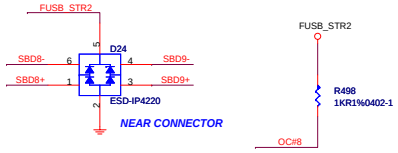


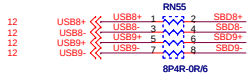




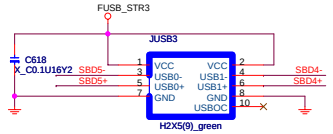
FRONT USB PORT 8,9

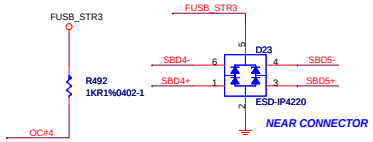






FRONT USB PORT 4,5





MSI MICRO-START INT'L CO.,LTD.		
Title: Front USB Connectors		
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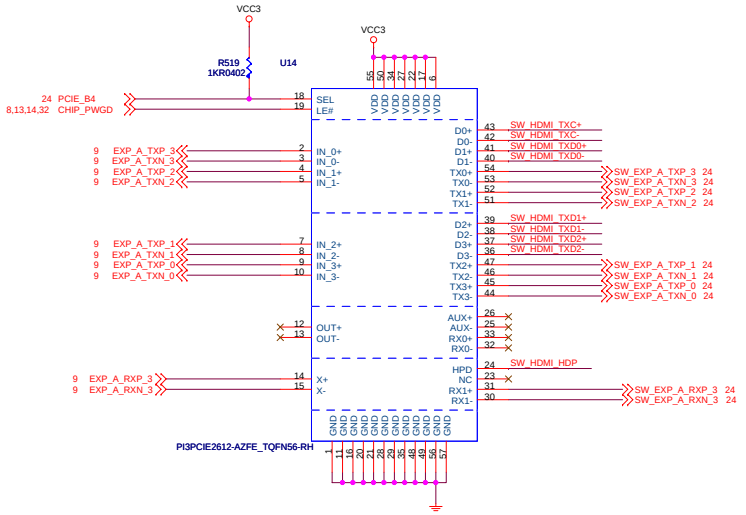
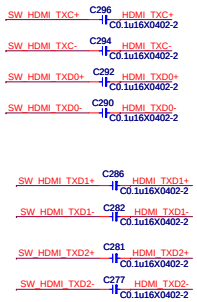
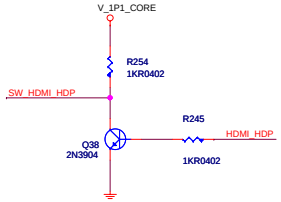
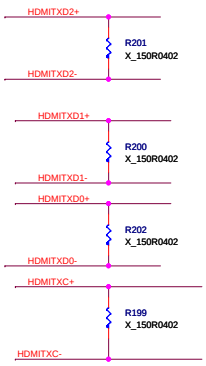
EMI Solution

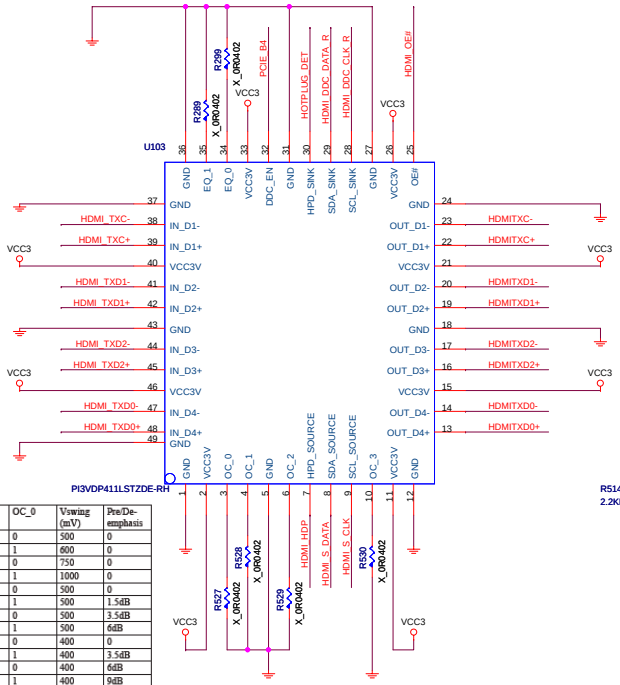


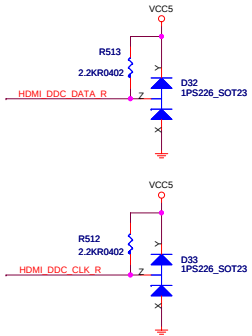


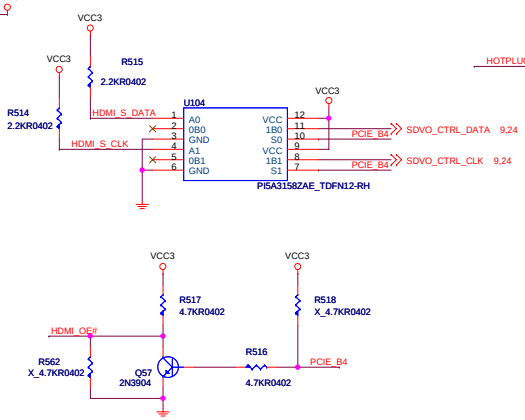


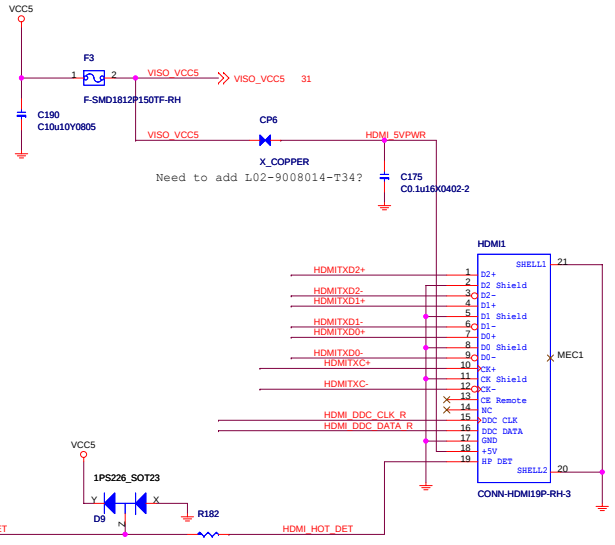


Close to Connector









N5I-19M0161-S42

Truth Table 1

OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

Truth Table 2

EQ_0	EQ_1	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

Symbol	Parameter	Min	Nom	Max	Units
VCC3V	3.3V Power Supply	3.0	3.3	3.6	V
ICC	Max Current			100	mA

MSI MICRO-START INT'L CO.,LTD.

Title: HDMI

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C	MS-7524M1	0A

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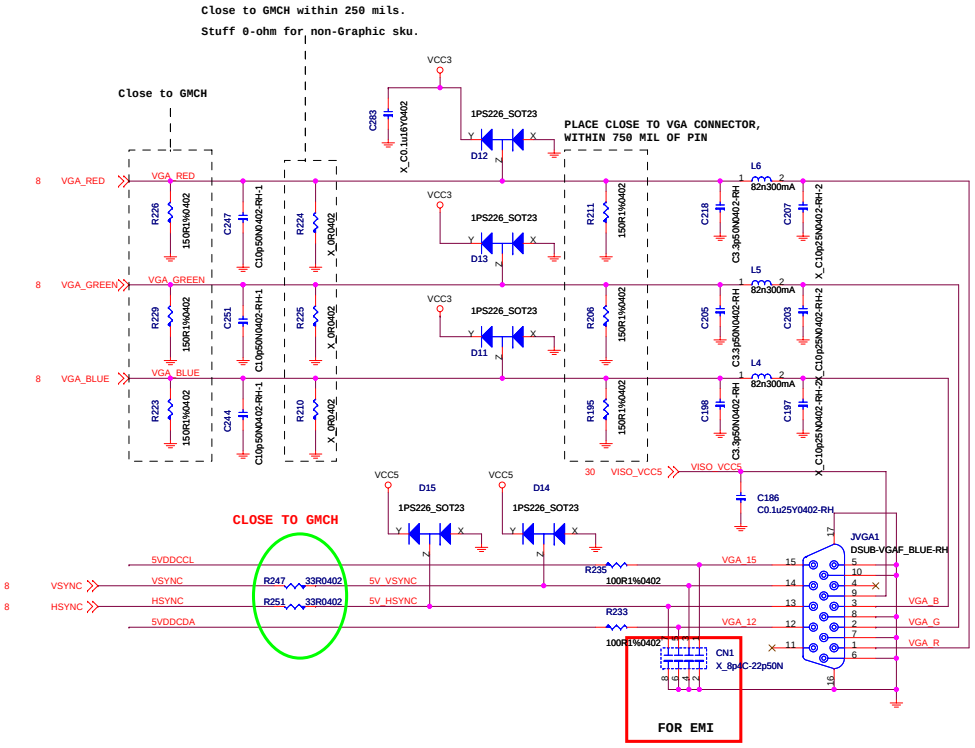

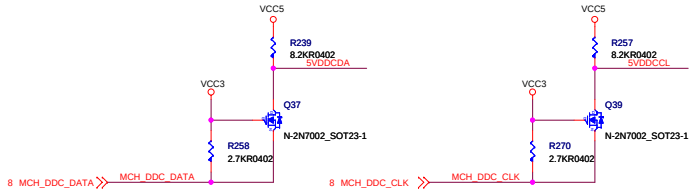

MSI MICRO-STAR INT'L CO.,LTD.

Title: VGA

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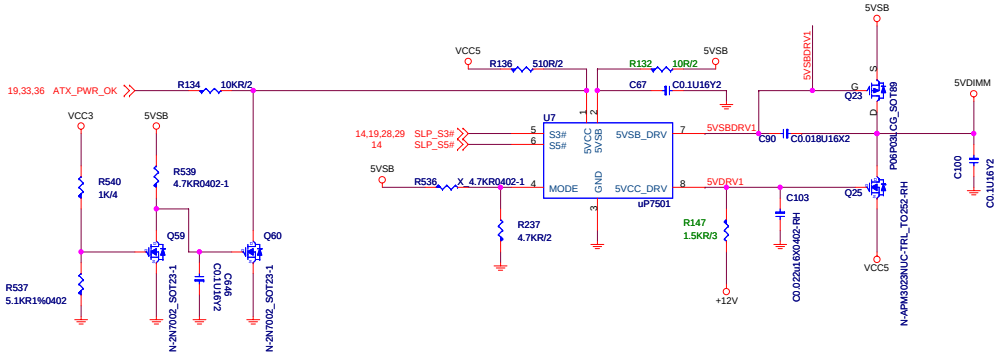
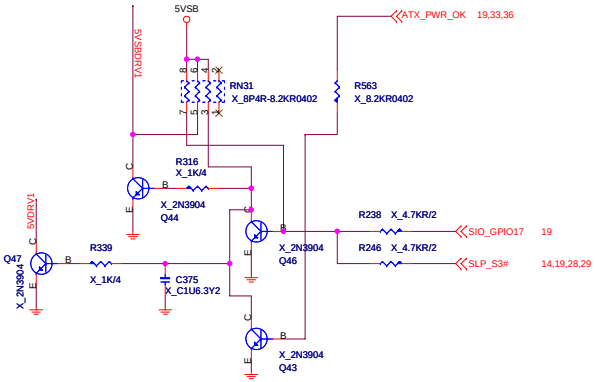
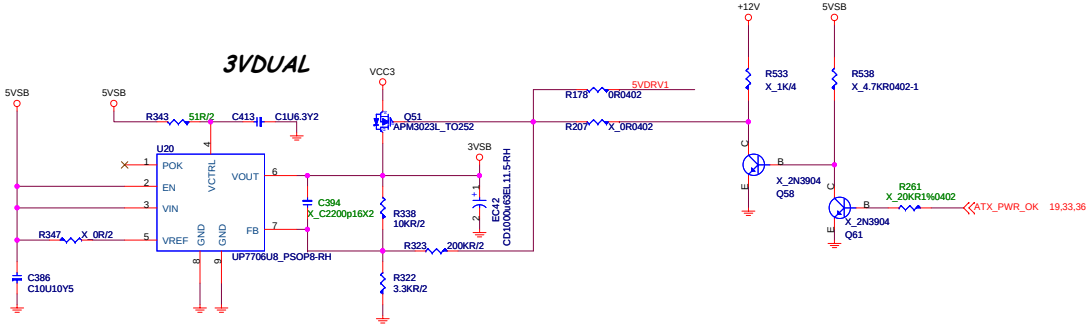
5VDIMM FOR DDR 9A



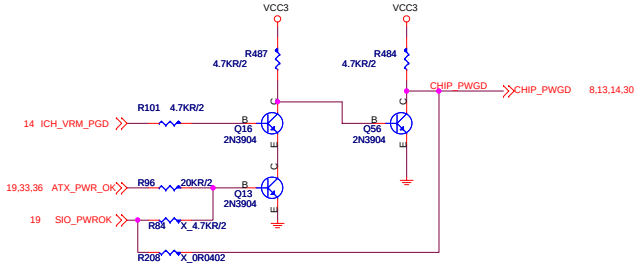


S5#	S3#	MODE	5VDUAL	Remarks
1	1	X	5VCC	S0/S1/S2 (Active)
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Shutdown	S4/S5

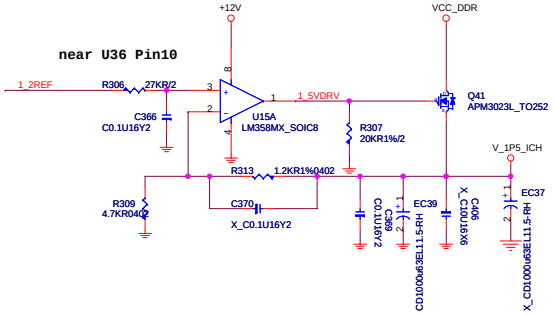
3VDUAL



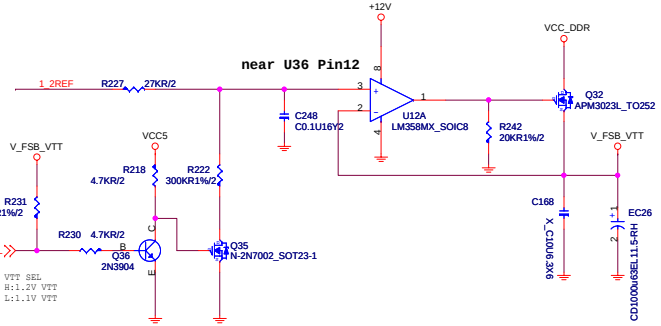
PWROK DELAY 100ms



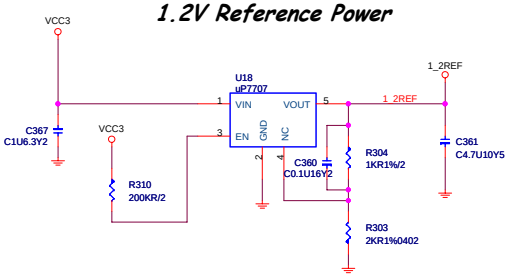
SB 1.5V 3.543A

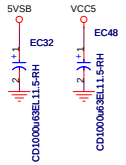


1.2V 6A



1.2V Reference Power





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Title: ACPI Controller UPI

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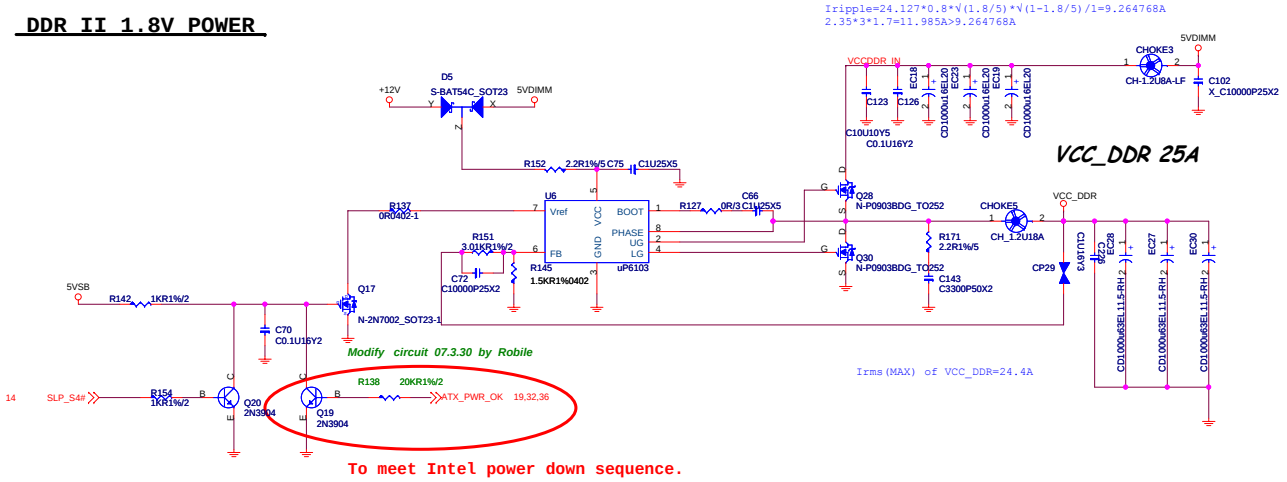
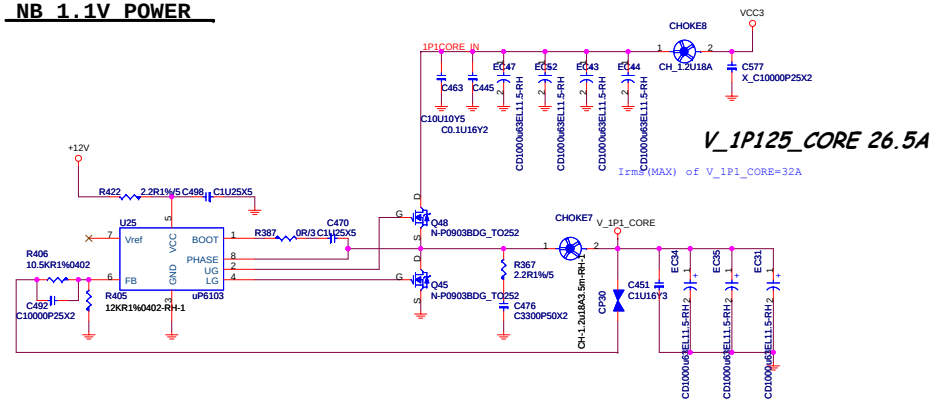
DDR II 1.8V POWER

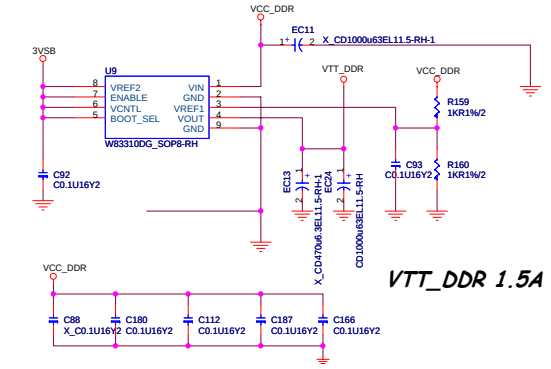


NB 1.1V POWER



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MSI MICRO-STAR INT'L CO.,LTD.

Title: NB Core & DDR Power

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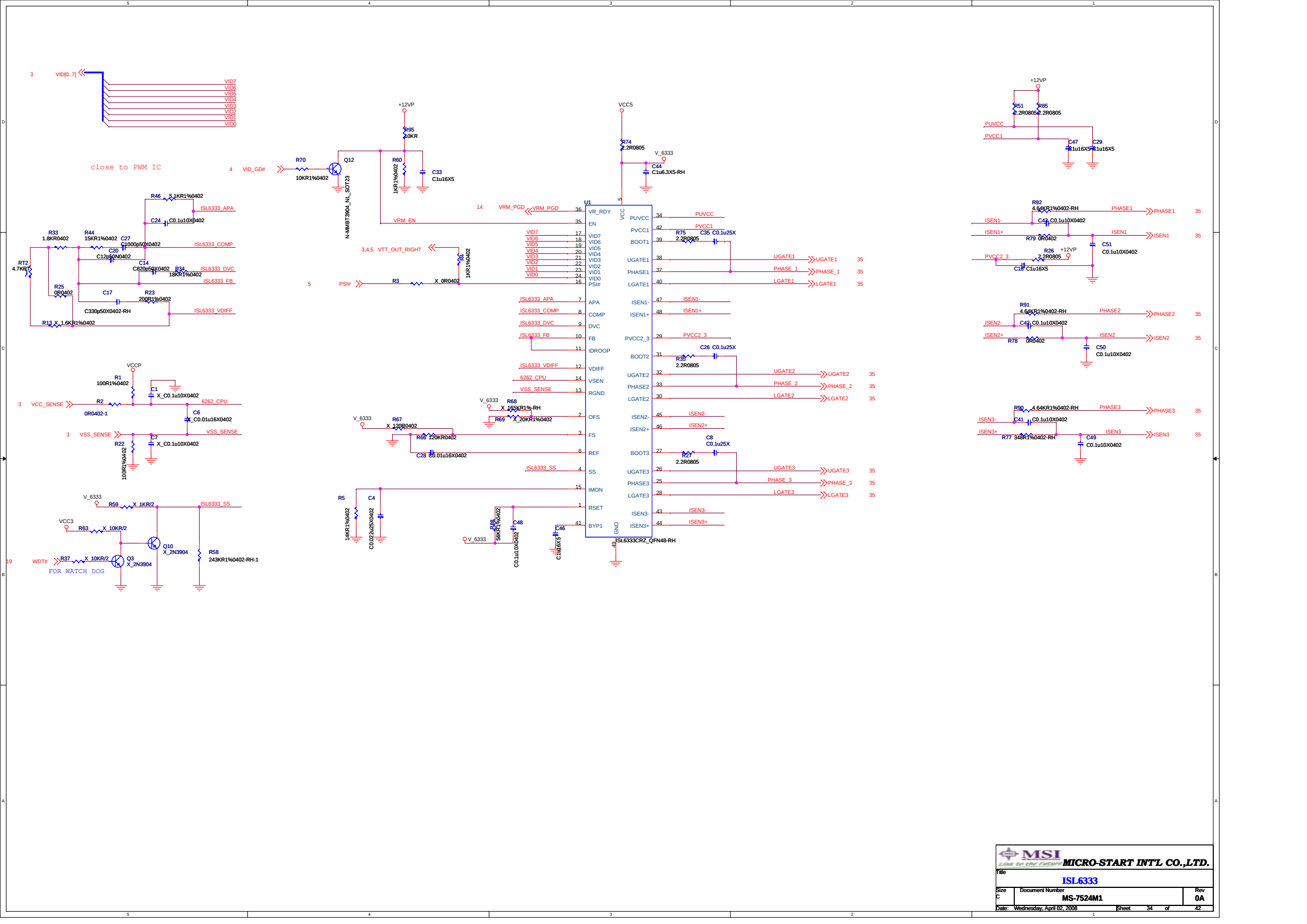

MSI MICRO-START INT'L CO.,LTD.

Title: ISL6333

Size	Document Number	Rev
C	MS-7524M1	0A

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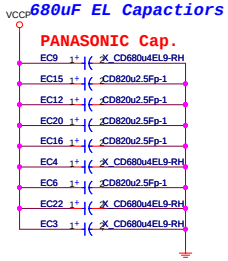
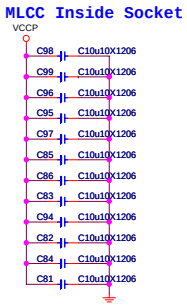
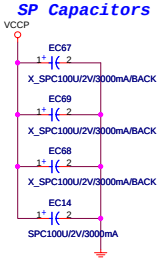
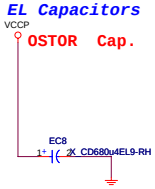
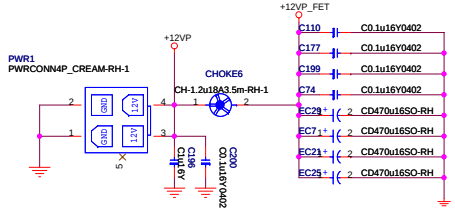


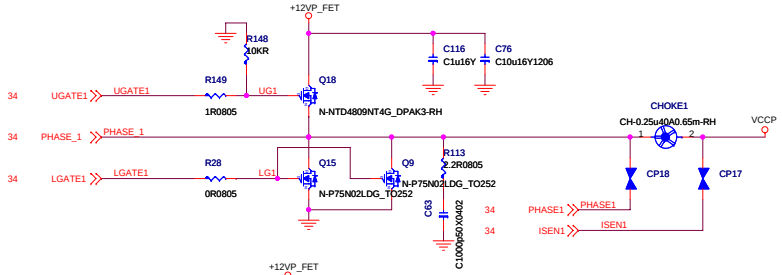


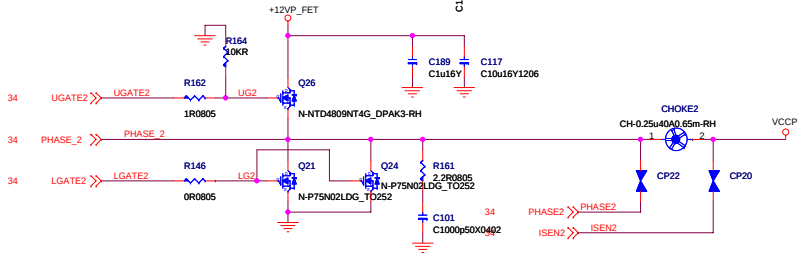


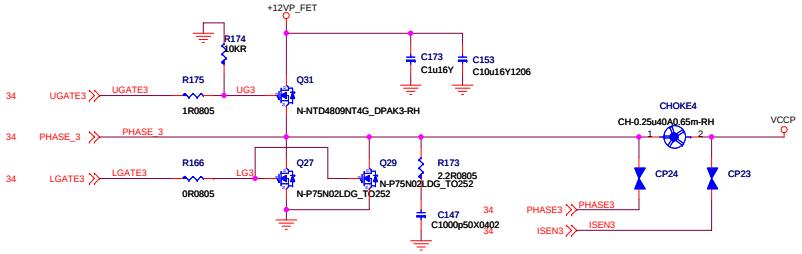




Part Number Description	Rated voltage (VDC)	Rated Capacitance (µF)	tanδ	Leakage Current (µA)	E S R 100-300kHz at 20°C (mΩ)	Rated ripple current 100kHz at105°C (mA r.m.s.)
APSC160E▭▭471MJB58	16	470	0.10	1504	10	6100







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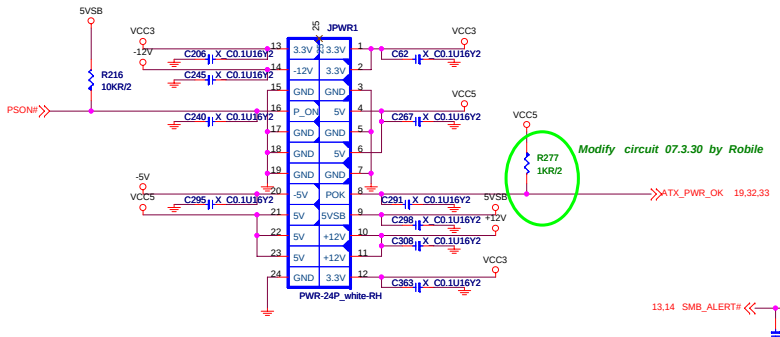
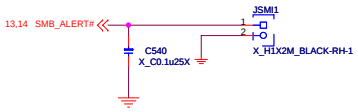
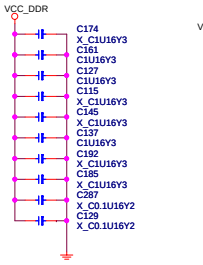
ATX POWER CONNECTOR

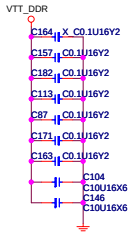


SMI

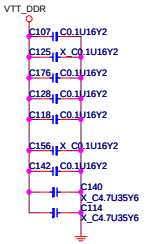


CHANNEL A V_SM_VTT DECOUPLING CAPS

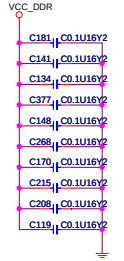


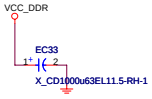


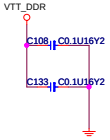
CHANNEL B V_SM_VTT DECOUPLING CAPS

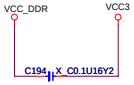


FOR EMI

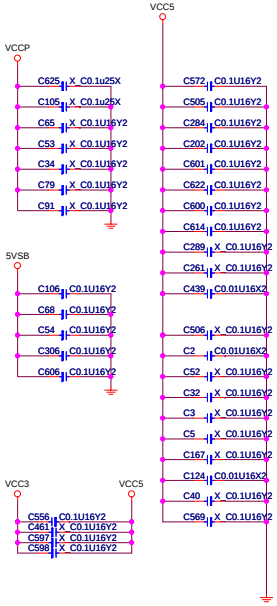


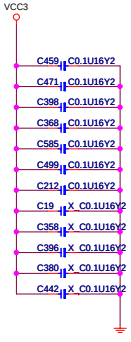


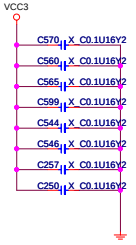


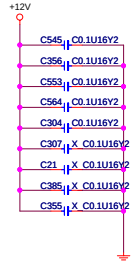


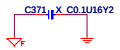
Cap. for EMI & Power

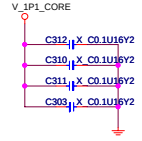


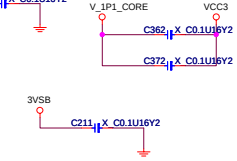


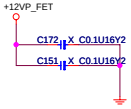


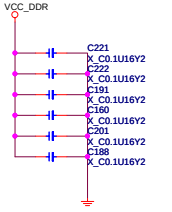




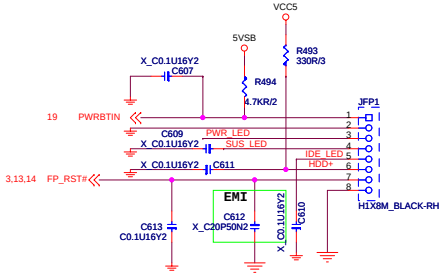


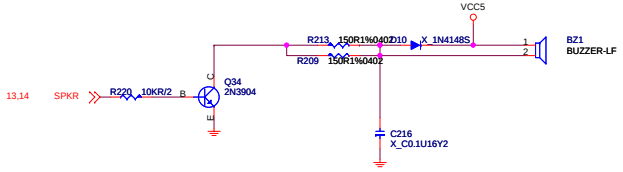




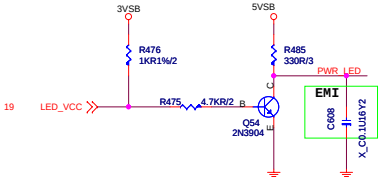


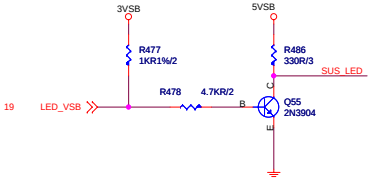
FRONT PANNEL

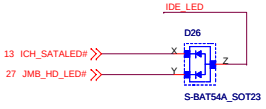




LED (for Fintek 71882)







MSI MICRO-START INT'L CO.,LTD.

Title: ATX Connector / F_Panel

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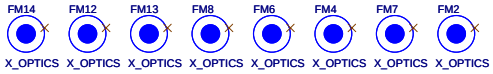
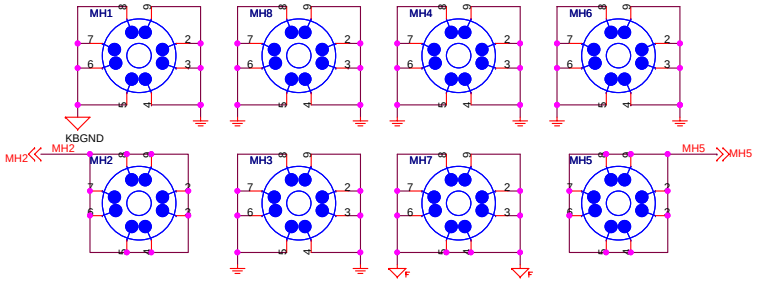
Optical Fiducial Marks-120

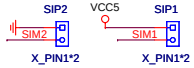
Optical Fiducial Marks-100

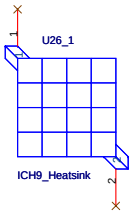


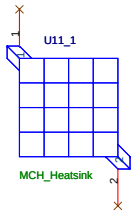
Mounting Holes



Simulation







MSI MICRO-START INT'L CO.,LTD.

Title: Manual & Option Parts

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